User's Guide

Publication Number E2409-97002
March 1998

For Safety Information, Warranties, and Regulatory Information, see the pages at the end of this manual.

HP E2409C Analysis Probe for Intel 80286

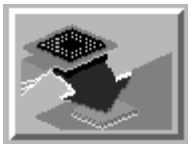
The HP E2409C Analysis Probe — At a Glance

The HP E2409C Analysis Probe provides a complete interface for state or timing analysis between any of the supported 80286 microprocessors listed below — or compatible chips by other manufacturers — and HP logic analyzers. The supported logic analyzers are listed in chapter 1.

Supported Microprocessors

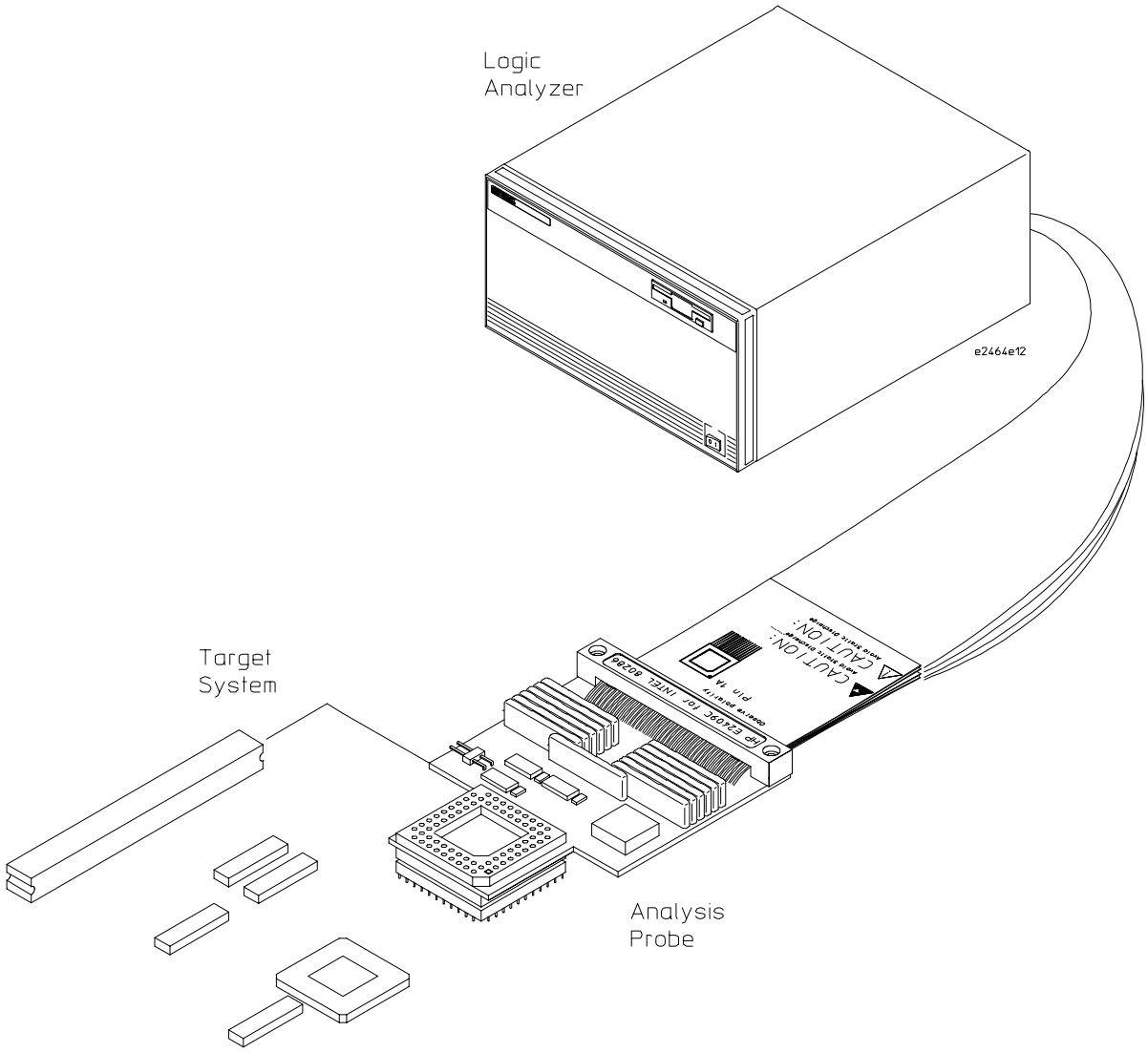
Microprocessor	Package	Ordering Information
80286	68-pin PGA	E2409C
80286	68-pin contact PLCC	E2409C option 1CB

The analysis probe provides the physical connection between the target microprocessor and the logic analyzer. The configuration software on the enclosed disks set up the logic analyzer for compatibility with the analysis probe. The inverse assemblers on the disks let you obtain displays of the 80286 data bus in 80286 assembly language mnemonics.



If you are using the analysis probe with the HP 16600 or HP 16700 series logic analysis systems, you only need this manual as a reference. The HP 16600 and 16700 series contain a Setup Assistant, which guides you through the connection and configuration process using onscreen dialog windows. For an overview of Setup Assistant, refer to Chapter 1, "Setup Assistant."

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manuals for those products.

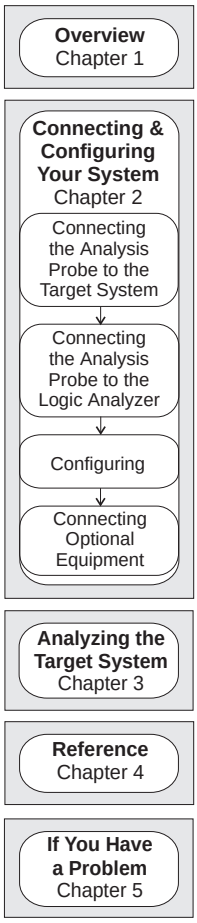


Analyzing a Target System with the HP E2409C Analysis Probe

In This Book

This book is the User's Guide for the HP E2409C Analysis Probe. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This user's guide is organized into the following chapters:



Chapter 1 contains overview information, including a list of required equipment.

Chapter 2 explains how to connect the logic analyzer to your target system through the analysis probe, and how to configure the analysis probe and logic analyzer to interpret target system activity. The last section in this chapter shows you how to hook up optional equipment to obtain additional functionality.

HP 16600 and HP 16700 Series Logic Analysis Systems

If you are using the analysis probe with HP 16600 or HP 16700 series logic analysis systems, you only need this manual as a reference for obtaining and interpreting data. The HP 16600 and HP 16700 contain a Setup Assistant, which guides you through the connection and configuration process using onscreen dialog windows. For an overview of Setup Assistant, refer to chapter 1, "Setup Assistant."

Chapter 3 provides information on analyzing the supported microprocessors.

Chapter 4 contains reference information on the analysis probe.

Chapter 5 contains troubleshooting information.

Contents

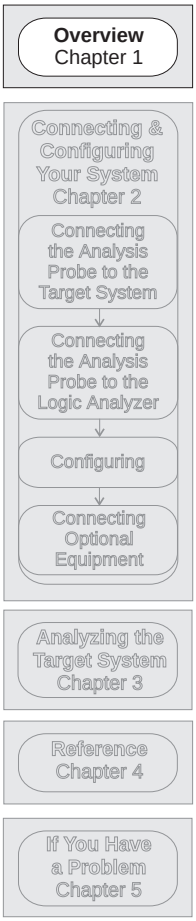
1

Overview

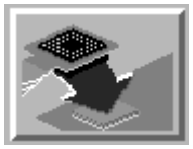
Overview

This chapter describes:

- Setup Assistant
- Logic analyzers supported
- Logic analyzer software version requirements
- Equipment used with the analysis probe
- Equipment supplied
- Minimum equipment required
- Additional equipment supported



Setup Assistant



Setup Assistant is an online tool for connecting and configuring your logic analysis system for microprocessor and bus analysis. Setup Assistant is available on the HP 16600 and HP 16700 series logic analysis systems. You can use Setup Assistant in place of the connection and configuration procedures provided in chapter 2.

This menu-driven tool will guide you through the connection procedures for connecting the logic analyzer to an analysis probe, an emulation module, or other supported equipment. It will also guide you through connecting an analysis probe to the target system.

Access Setup Assistant by clicking its icon in the Logic Analysis System window. The on-screen dialog prompts you to choose the type of measurements you want to make, the type of target system, and the associated products that you want to set up.

If you ordered this product with your HP 16600/700 logic analysis system, the logic analysis system has the latest software installed, including support for this product. If you received this product after you received your logic analysis system, this product might not be listed under supported products. In that case, you need to install the I80286 Processor Support Package. Use the procedure on the CD-ROM jacket to install the I80286 Processor Support Package.

Logic Analyzers Supported

The table below lists the logic analyzers supported by the HP E2409C analysis probe. Logic analyzer software version requirements are shown on the following page.

The HP E2409C requires three logic analyzer pods (51 channels) for inverse assembly. The analysis probe contains one additional pod that you can monitor.

Logic Analyzers Supported

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
16600A	204	100 MHz	125 MHz	64 k states
16601A	136	100 MHz	125 MHz	64 k states
16602A	102	100 MHz	125 MHz	64 k states
16603A	68	100 MHz	125 MHz	64 k states
16550A (one card)	102/card	100 MHz	250 MHz	4 k states
16554A (one card)	68/card	70 MHz	125 MHz	512 k states
16555A (one card)	68/card	110 MHz	250 MHz	1 M states
16555D (one card)	68/card	110 MHz	250 MHz	2 M states
16556A (one card)	68/card	100 MHz	200 MHz	1 M states
16556D (one card)	68/card	100 MHz	200 MHz	2 M states
1660A/AS/C/CS/CP	136	100 MHz	250 MHz	4 k states
1661A/AS/C/CS/CP	102	100 MHz	250 MHz	4 k states
1662A/AS/C/CS/CP	68	100 MHz	250 MHz	4 k states
1670A	136	70 MHz	125 MHz	64 k or .5 M states
1670D	136	100 MHz	125 MHz	64 k or 1 M states
1671A	102	70 MHz	125 MHz	64 k or .5 M
1671D	102	100 MHz	125 MHz	64 k or 1 M
1672A	68	70 MHz	125 MHz	64 k or .5 M
1672D	68	100 MHz	125 MHz	64 k or 1 M

Logic analyzer software version requirements

The logic analyzers must have software with a version number greater than or equal to those listed below to make a measurement with the HP E2409C. You can obtain the latest software at the following web site:

www.hp.com/go/logicanalyzer

If your software version is older than those below, load new system software with the listed version numbers or higher before loading the HP E2409C software.

Logic Analyzer Software Version Requirements

Logic Analyzer	Minimum Logic Analyzer Software Version for use with HP E2409C
HP 16600 Series	The latest HP 16600 logic analyzer software version is on the CD-ROM shipped with this product.
HP 1660A/AS Series	A.03.01
HP 1660C/CS/CP Series	A.02.01
HP 1670A/D Series	A.02.01
Mainframes*	
HP 16700 Series	The latest HP 16700 logic analyzer software version is on the CD-ROM shipped with this product.
HP 16500C Mainframe	A.01.05
HP 16500B Mainframe	A.03.14

* The mainframes are used with the HP 16550 and HP 16554/55/56 logic analyzer modules.

Equipment Used with the Analysis Probe

This section lists equipment used with the analysis probe. This information is organized under the following titles: equipment supplied, minimum equipment required, and additional equipment supported

Equipment supplied

The equipment supplied with the analysis probe is shown in the illustration on the next page. It is listed below:

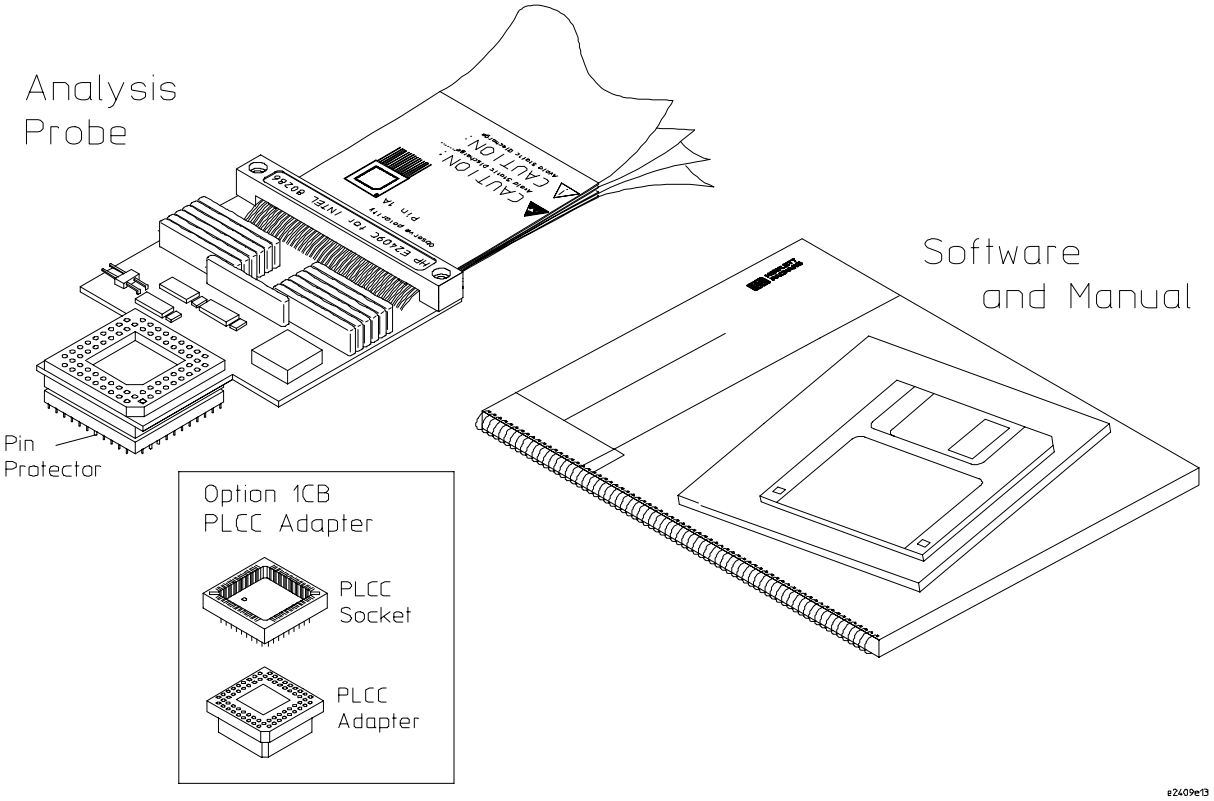
HP E2409C

- The analysis probe, which includes the analysis probe circuit card and cables.
- Logic analyzer configuration files and inverse assembler software on a 3.5-inch disk.
- Logic analyzer configuration files and inverse assembler software on a CD-ROM.
- One pin protector/adapter.
- This User's Guide.

HP E2409C option 1CB

If you ordered option 1CB, you received the following additional equipment:

- PLCC adapter
- PLCC socket



Equipment Supplied with the HP E2409C

Minimum equipment required

For state and timing analysis of an 80286 target system, you need all of the following items.

- The HP E2409C Analysis Probe.
- For 68-pin PLCC target systems, the E2409C option 1CB.
- One of the logic analyzers listed on page 1-4. The logic analyzer software version requirements are listed on page 1-5.

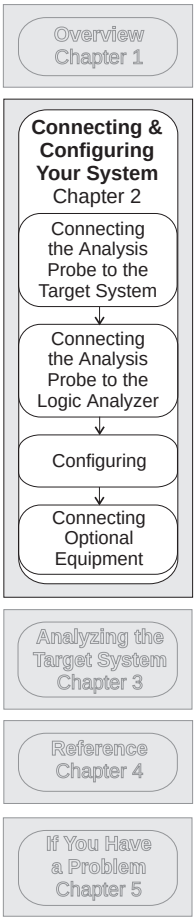
Additional equipment supported

The HP E2409C does not support any additional equipment.

2

Connecting and Configuring Your System

Connecting and Configuring Your System

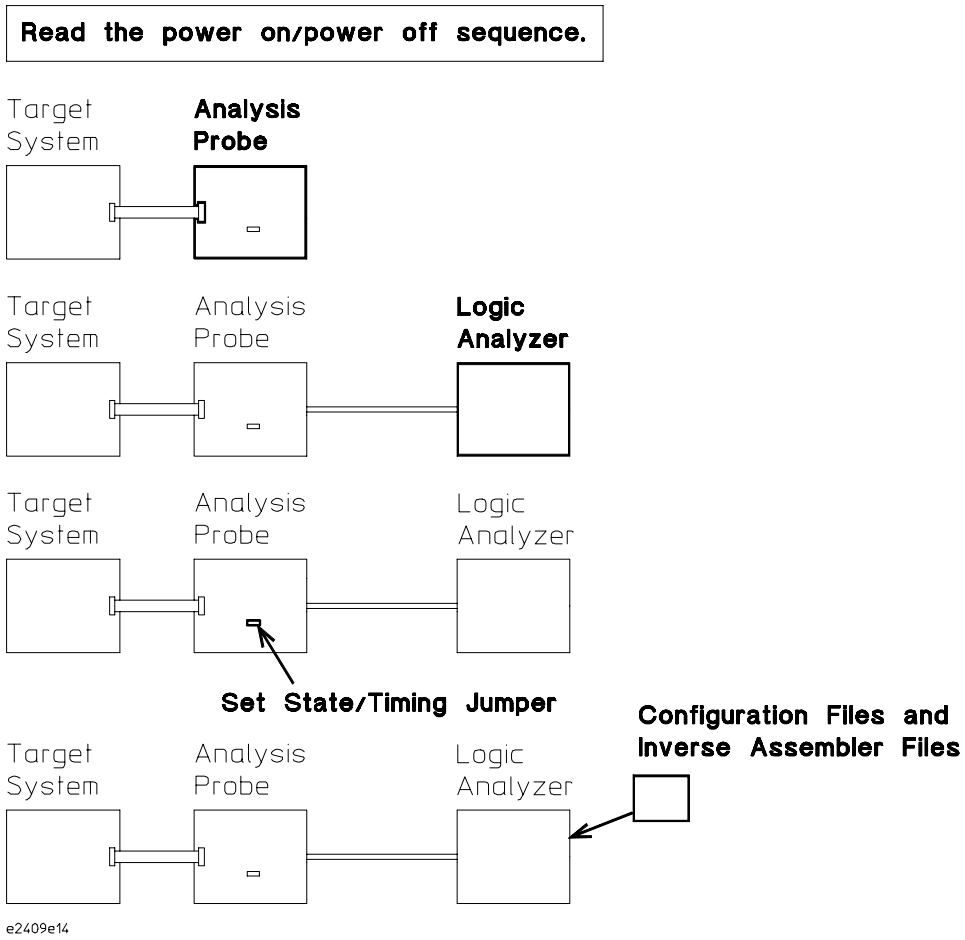


This chapter shows you how to connect the logic analyzer to the target system through the analysis probe.

If you are connecting to an HP 16600 or HP 16700 series logic analysis system, follow the instructions given onscreen in the Setup Assistant for connecting and configuring your system. Use this manual for additional information, if desired. Refer to chapter 1 for a description of Setup Assistant.

If you are not using the Setup Assistant, follow the instructions given in this chapter. This chapter is divided into the following sections; the order shown here is the recommended order for performing these tasks:

- Read the power on/power off sequence
- Connect the analysis probe to the target system
- Connect the analysis probe to the logic analyzer
- Configure the analysis probe
- Configure the logic analyzer
- Connect optional equipment



Connection Sequence

Power-on/Power-off Sequence

Listed below are the sequences for powering on and off a fully connected system. Simply stated, your target system is always the last to be powered on, and the first to be powered off.

To power on HP 16600 and HP 16700 series logic analysis systems

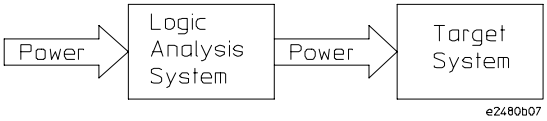
Ensure the target system is powered off.

1. Turn on the logic analyzer. The Setup Assistant will guide you through the process of connecting and configuring the analysis probe.
2. When the analysis probe is connected to the target system and logic analyzer, and everything is configured, turn on your target system.

To power on all other logic analyzers

With all components connected, power on your system in the following order:

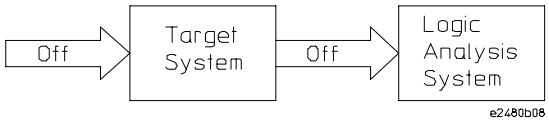
1. Logic analysis system.
2. Your target system.



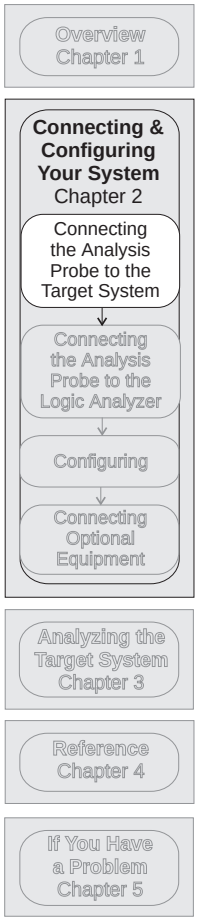
To power off

Turn off power to your system in the following order:

1. Turn off your target system.
2. Turn off your logic analysis system.



Connecting the Analysis Probe to the Target System



This section explains how to connect the HP E2409C Analysis Probe to the target system. Connecting the analysis probe to the target system consists of the following tasks:

- For PGA target systems, connect the analysis probe directly to the target system.

  Refer to "To connect to a PGA target system."
- For PLCC target systems, connect the adapter socket to the target system.

  Refer to "To connect to a PLCC target system."
- For PLCC target systems, connect the analysis probe to the adapter.

The remainder of this section describes these general tasks in more detail.

Protect Your Equipment

The analysis probe socket assembly pins are covered for shipment with a conductive foam wafer or conductive plastic pin protector. This is done to protect the delicate gold-plated pins from damage due to impact. When you are not using the analysis probe, protect the socket assembly pins from damage by covering them with the pin protector.

To connect to a PGA target system

CAUTION

Equipment Damage. To prevent equipment damage, remove power from the target system and make sure no logic analyzer cables are connected to the analysis probe.

1. Turn off the target system and disconnect all logic analyzer cables from the analysis probe.
2. Remove the 80286 microprocessor from its socket on the target system and store it in a protected environment.
3. Prior to inserting the analysis probe PGA connector in the target system socket, note the position of pin 1 on the analysis probe connector and the target system socket (refer to the figure on next page).
4. Carefully align the analysis probe connector with the socket on the target system so that all pins are making contact.

CAUTION

Serious damage to the target system or analysis probe can result from incorrect connection. Ensure that pin 1 on the analysis probe and the target system are aligned, and that all pins are making contact.

6. Plug the analysis probe connector into the microprocessor socket on the target system.

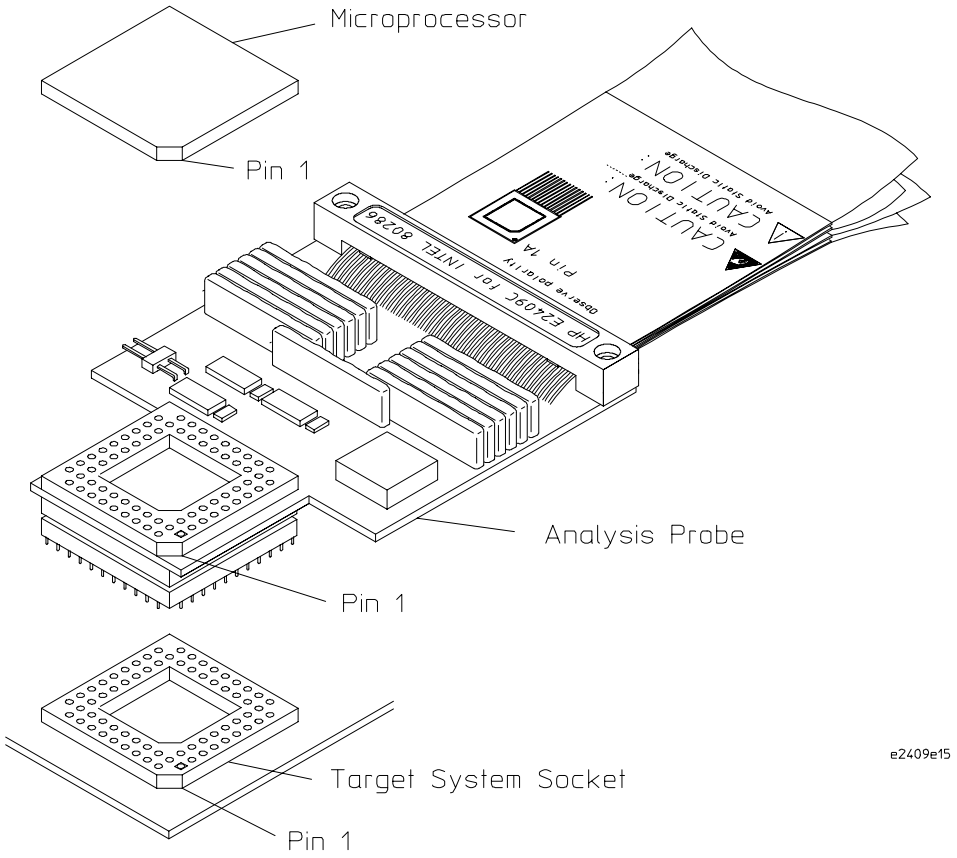
   If the analysis probe circuit board interferes with components of the target system or if a higher profile is required, insert additional plastic pin protectors. You can order plastic pin protectors from Hewlett-Packard using the part number 1200-1516. However, any 68-pin PGA IC socket with an 80286 footprint and gold-plated pins can be used.

7. Plug the 80286 microprocessor into the socket of the analysis probe board.

   The socket on the analysis probe board is designed with low-insertion-force pins to allow you to install or remove the microprocessor with a minimum amount of force.

CAUTION

Do not use sharp objects or excessive force when removing a microprocessor or socket from the analysis probe board. Traces on the analysis probe board may be damaged.



Pin 1 Location

To connect to a PLCC target system

The option 1CB PLCC adapter provides a connection between the analysis probe and the 68-pin 80286 PLCC microprocessor. The PLCC adapter attaches to the target system PLCC socket. The analysis probe PGA pins connect to the adapter socket. Option 1CB consists of the following:

- PLCC adapter
- PLCC socket

Use the following procedure to connect to a PLCC target system.

1 Using a PLCC extractor tool, remove the 80286 microprocessor from the PLCC socket on the target system.

CAUTION Be careful not to damage the PLCC socket or the microprocessor when removing the microprocessor from the target system.

2 Store the microprocessor in a protected environment.

CAUTION Serious damage to the target system or analysis probe can result from incorrect connection. Ensure that pin 1 on the analysis probe, PLCC adapter, and the target system are aligned, and that all pins are making contact.

3 Noting the position of pin 1, place the PLCC adapter in the microprocessor socket of the target system (refer to the figure on next page).

4 Plug the analysis probe connector into the PLCC adapter.

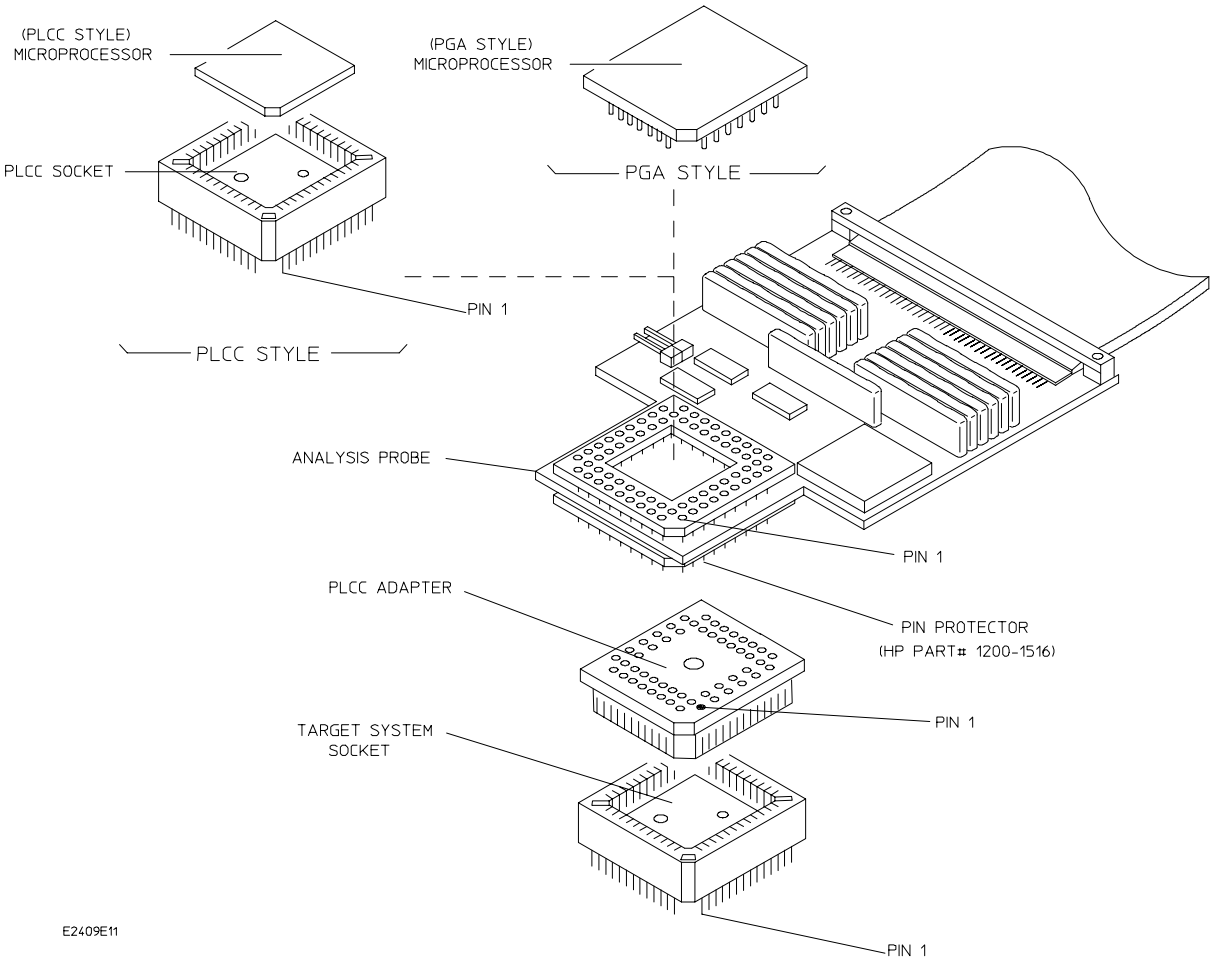
If the analysis probe circuit board interferes with components of the target system or if a higher profile is required, insert additional plastic pin protectors. You can order plastic pin protectors from Hewlett-Packard using the part number 1200-1516. However, any 68-pin PGA IC socket with an 80286 footprint and gold-plated pins can be used.

5 Using one of the following methods, install the 80286 microprocessor.

a If a PGA-style 80286 microprocessor is available, note the location of pin 1 on the microprocessor and the analysis probe socket and insert the PGA microprocessor in the socket on top of the analysis probe.

b If a PGA microprocessor is not available, note the location of pin 1 on the PLCC socket and the analysis probe socket, and install the PLCC socket on the analysis probe. Plug the PLCC microprocessor into the PLCC socket.

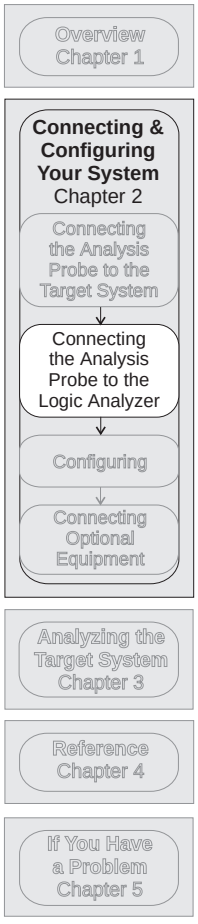
CAUTION To prevent pin damage and ensure proper connection, make sure the pins are aligned and seated correctly in the socket.



Installing the PLCC Adapter and PLCC Socket

> The PLCC socket adds additional capacitance to the circuit, but should not affect the performance of the microprocessor.

Connecting the Analysis Probe to the Logic Analyzer



The following sections show the connections between the logic analyzer pod cables and the analysis probe cables. Use the appropriate section for your logic analyzer. The configuration file names for each logic analyzer are located at the bottom of the connection diagrams.

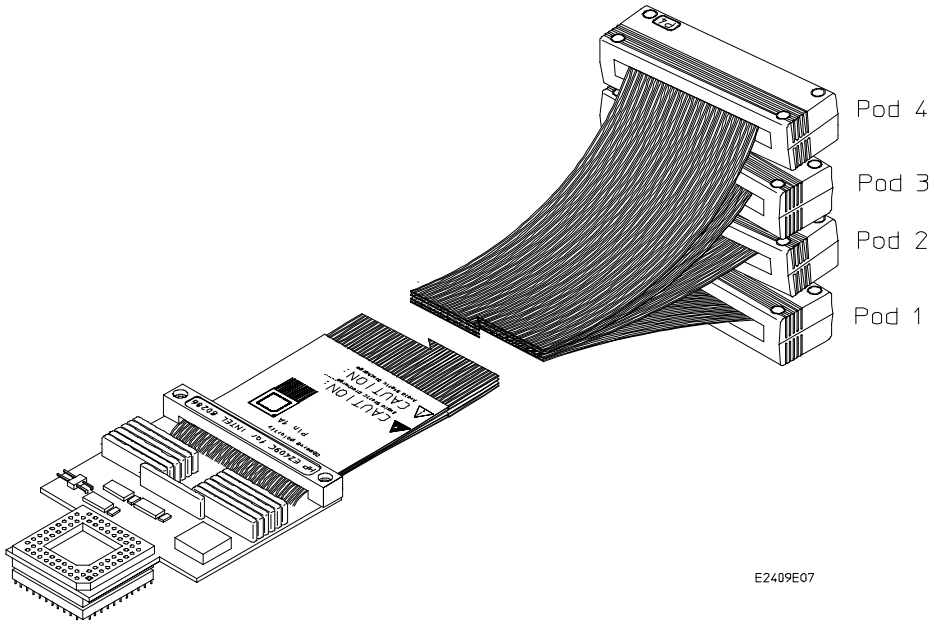
A minimum of three analysis probe pods are required for inverse assembly. A fourth pod contains additional signals you can monitor. The illustration on the following page shows the analysis probe pod locations.

This section shows connection diagrams for connecting the analysis probe to the logic analyzers listed below:

- HP 16600A logic analysis system
- HP 16601A logic analysis system
- HP 16602A logic analysis system
- HP 16603A logic analysis system
- HP 16550A logic analyzer (one card)
- HP 16554/55/56 logic analyzers (one card)
- HP 1660A/AS/C/CS/CP logic analyzers
- HP 1661A/AS/C/CS/CP logic analyzers
- HP 1662A/AS/C/CS/CP logic analyzers
- HP 1670A/D logic analyzers
- HP 1671A/D logic analyzers
- HP 1672A/D logic analyzers

Analysis probe pod locations

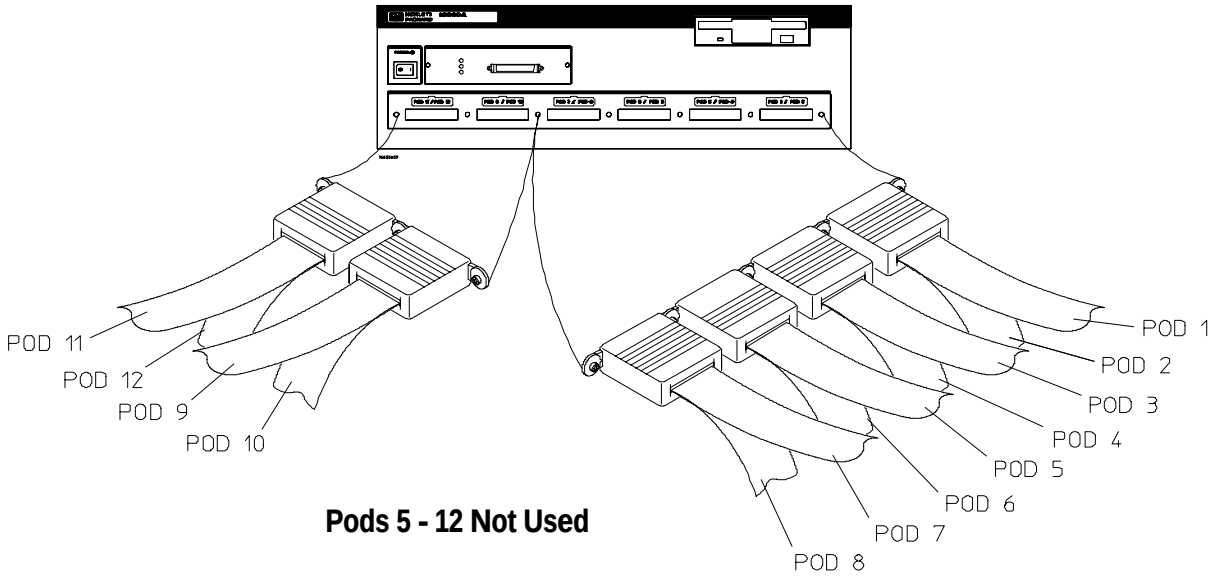
The illustration below shows the pod locations on the analysis probe.



HP E2409C Analysis Probe Pod Locations

To connect to the HP 16600A logic analysis system

Use the figure and table below to connect the analysis probe to the HP 16600A logic analysis system.

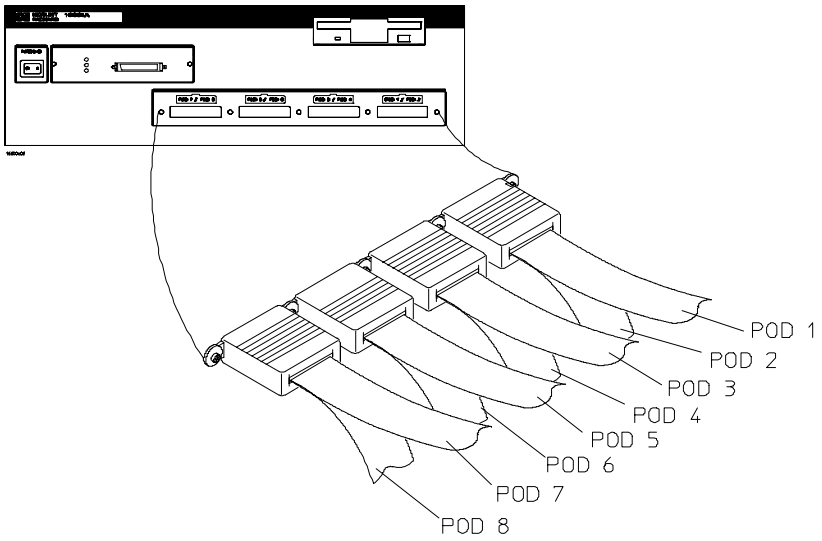


HP 16600	Pods 5 - 12	Pod 4	Pod 3	Pod 2	Pod 1
HP E2409C Connector	not used	P4 additional signals	P3 DATA	P2 ADDR/STAT	P1 ADDR clk ↑

Configuration File
Use configuration file C286_04 for the HP 16600 logic analysis system.

To connect to the HP 16601A logic analysis system

Use the figure and table below to connect the analysis probe to the HP 16601A logic analysis system.

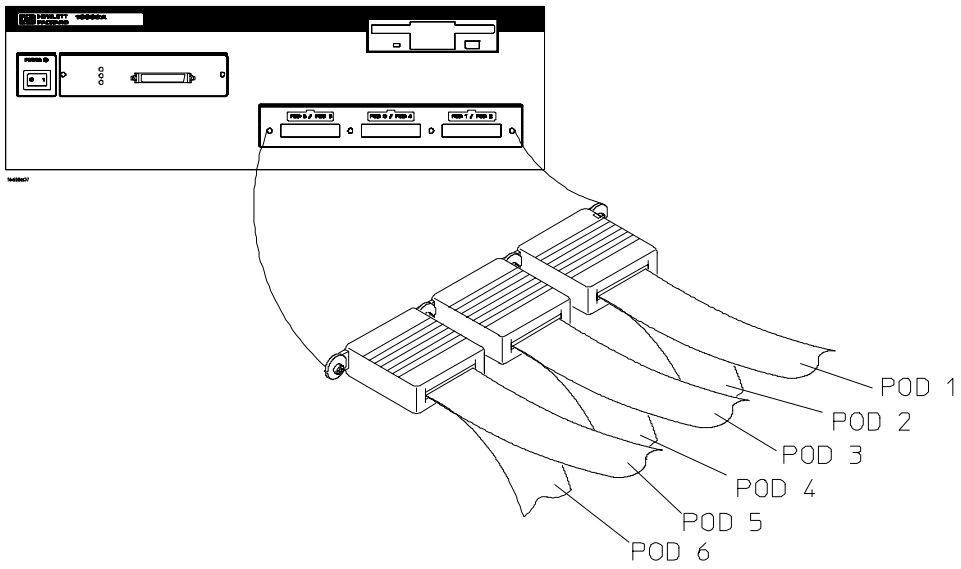


HP 16601	Pods 5 - 8	Pod 4	Pod 3	Pod 2	Pod 1
HP E2409C Connector	not used	P4 additional signals	P3 DATA	P2 ADDR/STAT	P1 ADDR clk ↑

Configuration File
Use configuration file C286_04 for the HP 16601 logic analysis system.

To connect to the HP 16602A logic analysis system

Use the figure and table below to connect the analysis probe to the HP 16602A logic analysis system.

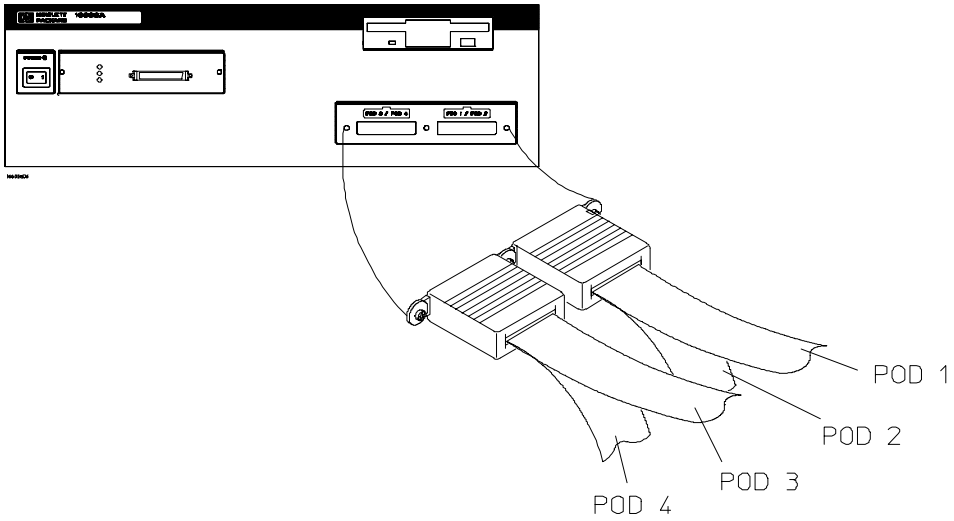


HP 16602	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2409C Connector	P6 not used	P5 not used	P4 additional signals	P3 DATA	P2 ADDR/STAT	P1 ADDR clk ↑

Configuration File
Use configuration file C286_04 for the HP 16602 logic analysis system.

To connect to the HP 16603A logic analysis system

Use the figure and table below to connect the analysis probe to the HP 16603A logic analysis system.

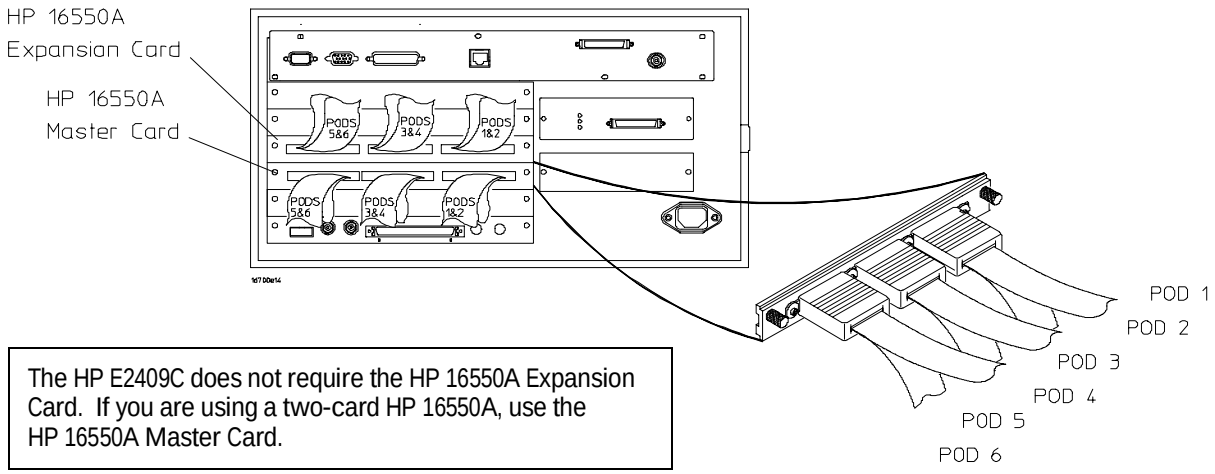


HP 16603	Pod 4	Pod 3	Pod 2	Pod 1
HP E2409C Connector	P4 additional signals	P3 DATA	P2 ADDR/STAT	P1 ADDR clk ↑

Configuration File
Use configuration file C286_04 for the HP 16603 logic analysis system.

To connect to the HP 16550A logic analyzer

Use the figure and table below to connect the analysis probe to the HP 16550A logic analyzer.



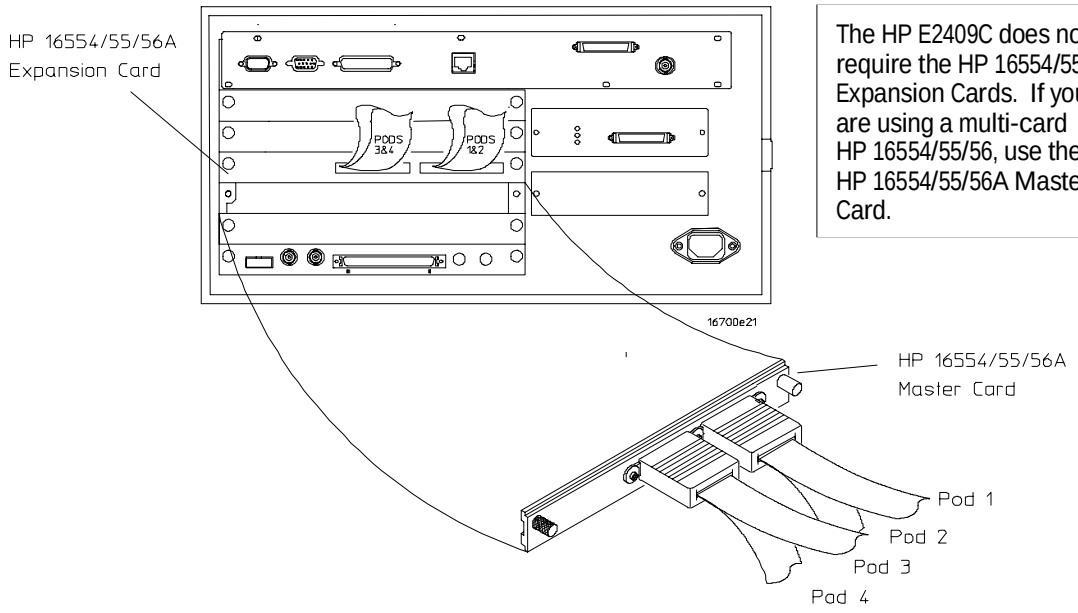
The HP E2409C does not require the HP 16550A Expansion Card. If you are using a two-card HP 16550A, use the HP 16550A Master Card.

HP 16550A Master Card	Master Card Pod 6	Master Card Pod 5	Master Card Pod 4	Master Card Pod 3	Master Card Pod 2	Master Card Pod 1
HP E2409C Connector	P6 not used	P5 not used	P4 additional signals	P3 DATA	P2 ADDR/STAT	P1 ADDR clk ↑

Configuration File
Use configuration file C286_04 for the HP 16550A logic analyzer.

To connect to the HP 16554/55/56 logic analyzers

Use the figure and table below to connect the analysis probe to the HP 16554A/55A/56A and HP 16555D/56D logic analyzers.



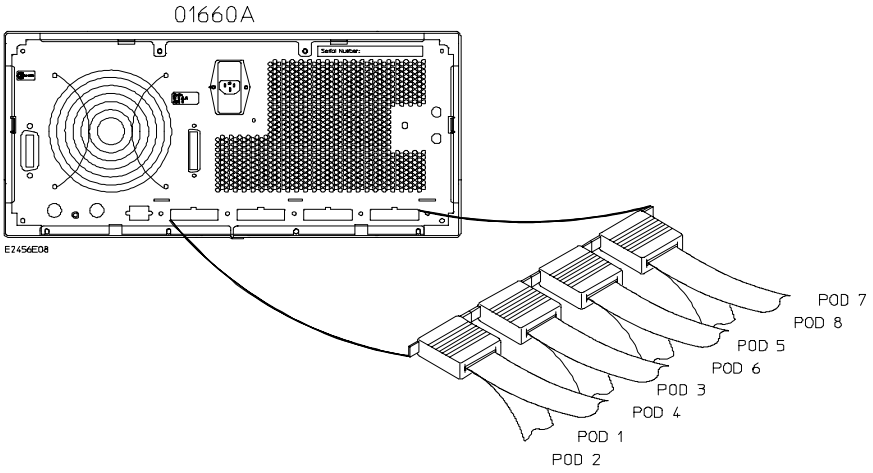
The HP E2409C does not require the HP 16554/55/56 Expansion Cards. If you are using a multi-card HP 16554/55/56, use the HP 16554/55/56A Master Card.

HP 16554/55/56 Master Card	Master Card Pod 4	Master Card Pod 3	Master Card Pod 2	Master Card Pod 1
HP E2409C Connector	P4 additional signals	P3 DATA	P2 ADDR/STAT	P1 ADDR clk ↑

Configuration File
Use configuration file C286_06 for the HP 16554/55/56 logic analyzers.

To connect to the HP 1660A/AS/C/CS/CP logic analyzers

Use the figure and table below to connect the analysis probe to the HP 1660A/C logic analyzers.

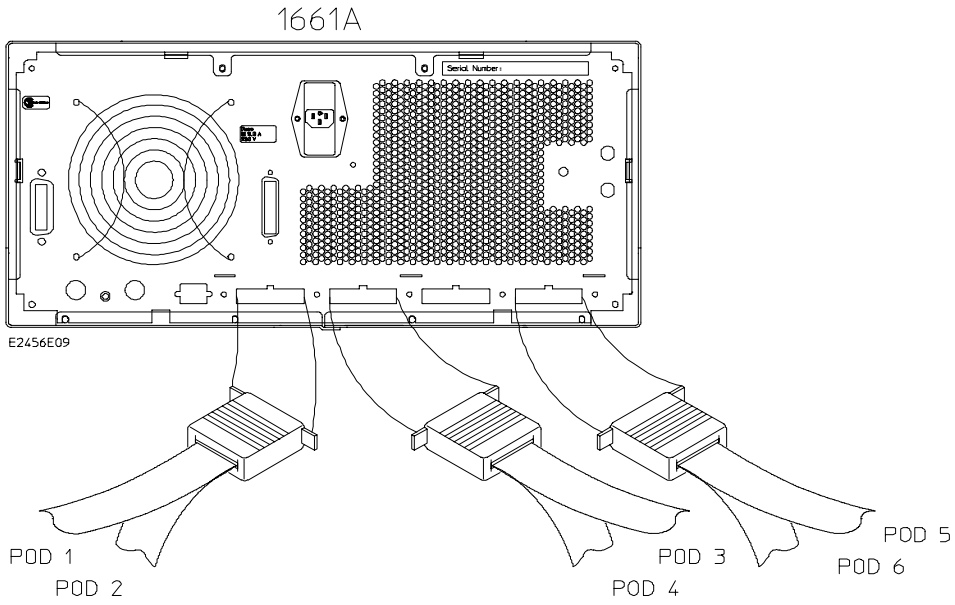


HP 1660A/C	Pod 1	Pod 2	Pod 3	Pod 4	Pods 5 - 8
HP E2409C Connector	P1 ADDR clk ↑	P2 ADDR/STAT	P3 DATA	P4 additional signals	not used

Configuration File
Use configuration file C286_05 for the HP 1660A/AS/C/CS/CP logic analyzers.

To connect to the HP 1661A/AS/C/CS/CP logic analyzers

Use the figure and table below to connect the analysis probe to the HP 1661A/C logic analyzers.

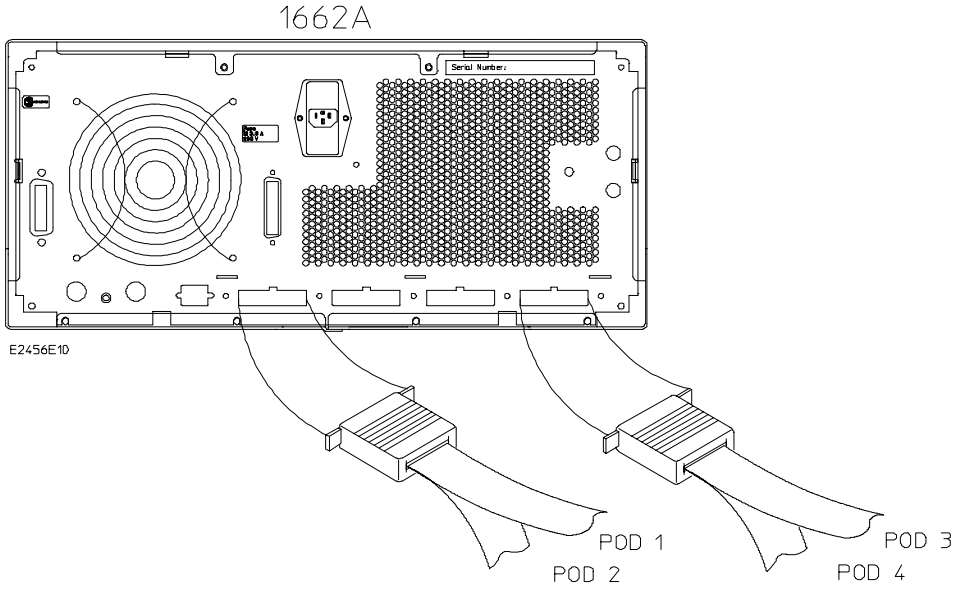


HP 1661A/C	Pod 1	Pod 2	Pod 3	Pod 4	Pod 5	Pod 6
HP E2409C Connector	P1 ADDR clk ↑	P2 ADDR/STAT	P3 DATA	P4 additional signals	P5 not used	P6 not used

Configuration File
Use configuration file C286_04 for the HP 1661A/AS/C/CS/CP logic analyzers.

To connect to the HP 1662A/AS/C/CS/CP logic analyzers

Use the figure and table below to connect the analysis probe to the HP 1662A/C logic analyzers.

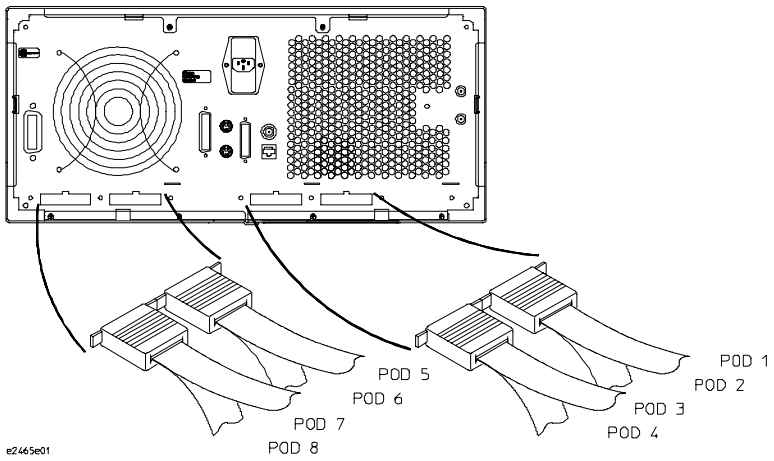


HP 1662A/C	Pod 1	Pod 2	Pod 3	Pod 4
HP E2409C Connector	P1 ADDR clk ↑	P2 ADDR/STAT	P3 DATA	P4 additional signals

Configuration File
Use configuration file C286_04 for the HP 1662A/AS/C/CS/CP logic analyzers.

To connect to the HP 1670A/D logic analyzer

Use the figure and table below to connect the analysis probe to the HP 1670A/D logic analyzers.

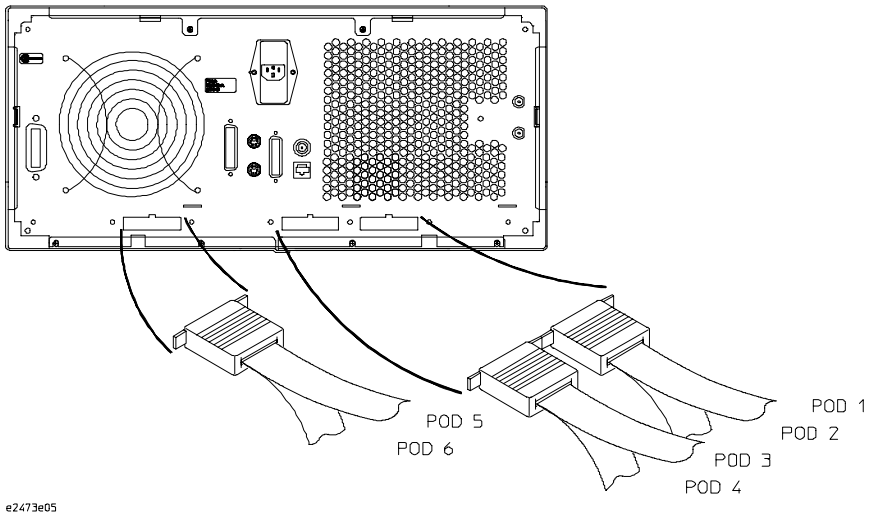


HP 1670A/D	Pods 5 - 8	Pod 4	Pod 3	Pod 2	Pod 1
HP E2409C Connector	not used	P4 additional signals	P3 DATA	P2 ADDR/STAT	P1 ADDR clk ↑

Configuration File
Use configuration file C286_05 for the HP 1670A/D logic analyzer.

To connect to the HP 1671A/D logic analyzer

Use the figure and table below to connect the analysis probe to the HP 1671A/D logic analyzer.

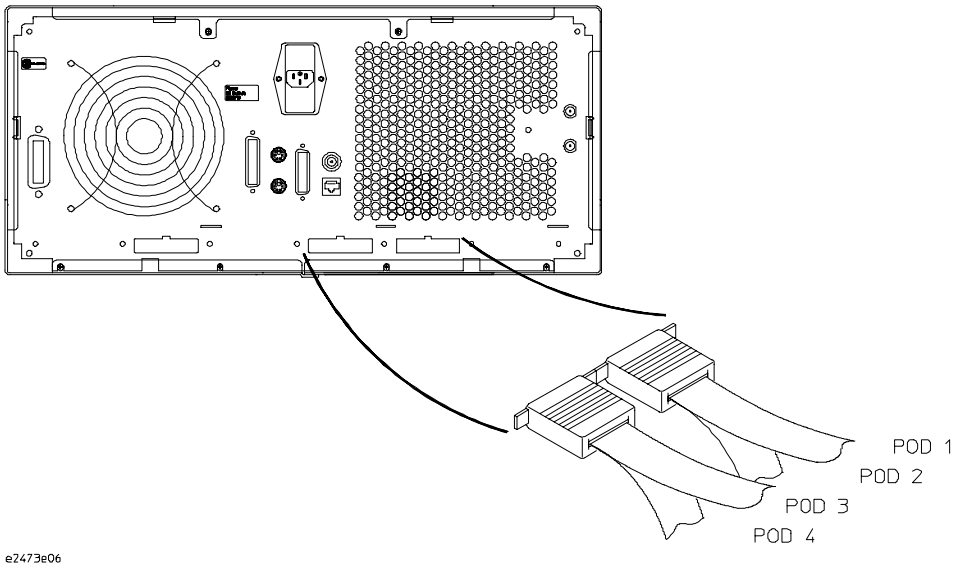


HP 1671A/D	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2409C Connector	not used	not used	P4 additional signals	P3 DATA	P2 ADDR/STAT	P1 ADDR clk ↑

Configuration File
Use configuration file C286_04 for the HP 1671A/D logic analyzer.

To connect to the HP 1672A/D logic analyzer

Use the figure and table below to connect the analysis probe to the HP 1672A/D logic analyzer.



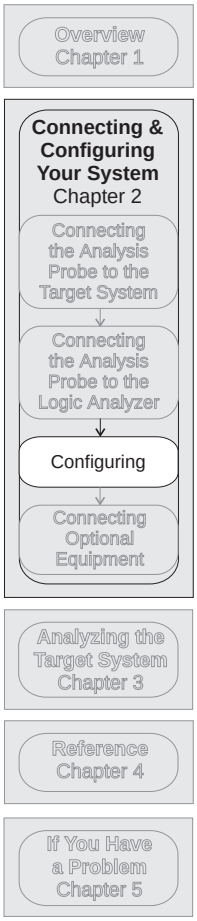
HP 1672A/D	Pod 4	Pod 3	Pod 2	Pod 1
HP E2409C Connector	P4 additional signals	P3 DATA	P2 ADDR/STAT	P1 ADDR clk ↑

Configuration File
Use configuration file C286_04 for the HP 1672A/D logic analyzer.

Configuring

This section shows you how to configure the HP E2409C Analysis Probe and the logic analyzer. It consists of the following tasks:

- Configuring the analysis probe
- Configuring the logic analyzer



Configuring the Analysis Probe

Configuring the analysis probe consists of setting the State/Timing jumper.

To set the State/Timing jumper

The analysis probe can operate in three modes: State-per-transfer, State-per-clock, or Timing. The State/Timing jumper selects the mode.

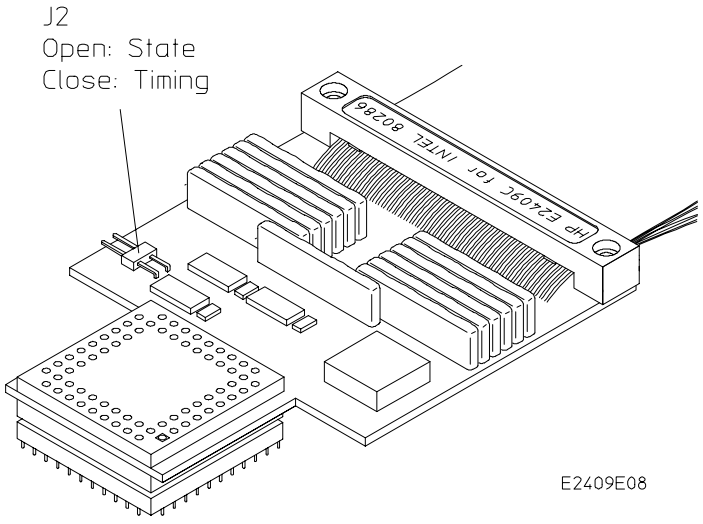
1 For State-per-transfer analysis, remove the State/Timing jumper at J2 (open).

In State-per-transfer mode, the active devices on the analysis probe latch and align the Address, Data, and Status bus.

2 For Timing or State-per-clock analysis, install the State/Timing jumper at J2 (closed).

In Timing mode, the active devices act as flow-through buffers. Inverse assembly is not available in Timing or State-per-clock modes.

See Chapter 3, "Modes of Operation" for additional information on the operating modes.



State/Timing Jumper Location

Configuring the Logic Analysis System

You configure the logic analyzer by loading a configuration file. The information in the configuration file includes:

- Label names and channel assignments for the logic analyzer
- Inverse assembler file name

The configuration file you use is determined by the logic analyzer you are using. The configuration file names are listed with the logic analyzer connection tables, and in a table at the end of this section.

The procedures for loading a configuration file depend on the type of logic analyzer you are using. There is one procedure for the HP 16600/700 series logic analysis systems, and another procedure for the HP 1660-series, HP 1670-series, and logic analyzer modules in an HP 16500B/C mainframe. Use the appropriate procedures for your analyzer.

To load configuration and inverse assembler files — HP 16600/700 logic analysis systems

If you did not use Setup Assistant, you can load the configuration and inverse assembler files from the logic analysis system hard disk.

1 Click on the File Manager icon. Use File Manager to ensure that the subdirectory /hplogic/configs/hp/i80286/ exists.

> If the above directory does not exist, you need to install the I80286 Processor Support Package. Close File Manager, then use the procedure on the CD-ROM jacket to install the I80286 Processor Support Package before you continue.

2 Using File Manager, select the configuration file you want to load in the /hplogic/configs/hp/i80286/ directory, then click Load. If you have more than one logic analyzer installed in your logic analysis system, use the Target field to select the machine you want to load.

The logic analyzer is configured for 80286 analysis by loading the appropriate configuration file. Loading this file also automatically loads the enhanced inverse assembler.

3 Close File Manager.

To load configuration and inverse assembler files — other logic analyzers

If you have an HP 1660-series, HP 1670-series, or logic analyzer modules in an HP 16500B/C mainframe use these procedures to load the configuration file and inverse assembler.

The first time you set up the analysis probe, make a duplicate copy of the master disk. For information on duplicating disks, refer to the reference manual for your logic analyzer.

For logic analyzers that have a hard disk, you might want to create a directory such as 80286 on the hard drive and copy the contents of the floppy onto the hard drive. You can then use the hard drive for loading files.

1. **Insert the floppy disk in the front disk drive of the logic analyzer.**
2. **Go to the Flexible Disk menu.**
3. **Configure the menu to load.**
4. **Use the knob to select the appropriate configuration file.**

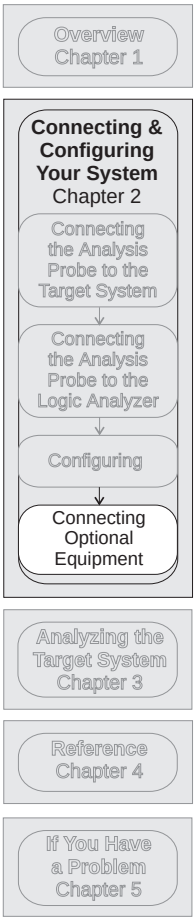
   Choosing the correct configuration file depends on which analyzer you are using. The configuration files are shown with the logic analyzer connection tables, and are also in the table on the next page.
5. **Select the appropriate analyzer on the menu. The HP 16500 logic analyzers are shown in the Logic Analyzer Configuration Files table.**
6. **Execute the load operation on the menu to load the file into the logic analyzer.**

   The logic analyzer is configured for 80286 analysis by loading the appropriate configuration file. Loading this file also automatically loads an inverse assembler. The configuration software checks the logic analyzer system during the load. If the logic analyzer has the appropriate software version, the configuration file automatically loads the enhanced inverse assembler.

Logic Analyzer Configuration Files

Analyzer Model	Analyzer Description (modules only)	Configuration File
16600A	na	C286_04
16601A	na	C286_04
16602A	na	C286_04
16603A	na	C286_04
16550A (one card)	100 MHz STATE 500 MHz TIMING	C286_04
16554A (one card)	0.5M SAMPLE 70/125 MHz LA	C286_06
16555A (one card)	1.0M SAMPLE 110/250 MHz LA	C286_06
16555D (one card)	2.0M SAMPLE 110/250 MHz LA	C286_06
16556A (one card)	1.0M SAMPLE 100/200 MHz LA	C286_06
16556D (one card)	2.0M SAMPLE 100/200 MHz LA	C286_06
1660A/AS/C/CS/CP	na	C286_05
1661A/AS/C/CS/CP	na	C286_04
1662A/AS/C/CS/CP	na	C286_04
1670A/D	na	C286_05
1671A/D	na	C286_04
1672A/D	na	C286_04

There is no additional optional equipment supported by the HP E2409C.

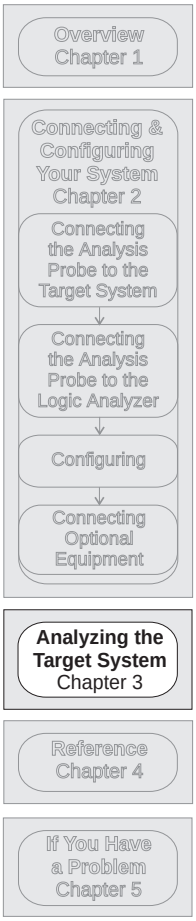


3

Analyzing the Target System

Analyzing the Target System

This chapter describes modes of operation for the HP E2409C Analysis Probe. It also describes analysis probe data, symbol encodings, and information about the inverse assemblers.



The information in this chapter is presented in the following sections:

- Modes of operation
- Logic analyzer configuration
- Using the inverse assemblers
- Coprocessor support

Modes of Operation

The HP E2409C Analysis Probe can be used in three different analysis modes: State-per-transfer, State-per-clock, and Timing. The following sections describe these operating modes and how to configure the logic analyzer for each mode.

State-per-transfer mode

In State-per-transfer mode, the analysis probe latches A[23:0] and D[15:0] only when there is a valid data transfer. This allows the logic analyzer to capture only valid data when it appears on the bus. The inverse assembly software reconstructs the 80286 mnemonic from the raw data. For State-per-transfer mode, the State/Timing jumper must be removed.

State-per-clock mode

In State-per-clock mode, a state is captured on every rising edge of the microprocessor clock, regardless of the validity of the bus cycle. To use State-per-clock mode, change the clock in the Format menu from J rising edge to K rising edge.

For State-per-clock mode, the State/Timing jumper must be installed, so that the latches on the analysis probe act like flow-through buffers. Inverse assembly is not supported in State-per-clock mode.

Timing mode

In Timing mode, the latches on the analysis probe act like flow-through buffers. The signals from the microprocessor go directly from the target system to the logic analyzer, with a 1-ns channel-to-channel skew. The skew for these signals relative to unbuffered signals is typically 5 ns.

To set up the analysis probe for timing, install the jumper to configure the analysis probe for Timing. Select the Configuration menu of the logic analyzer, the select the Type field for the analyzer, then select Timing.

Logic Analyzer Configuration

The following sections describe the logic analyzer configuration as set up by the configuration files.

Trigger specification

The trigger specification is set up by the software to store all states. If you modify the trigger specification to store only selected bus cycles, you may get incorrect or incomplete disassembly.

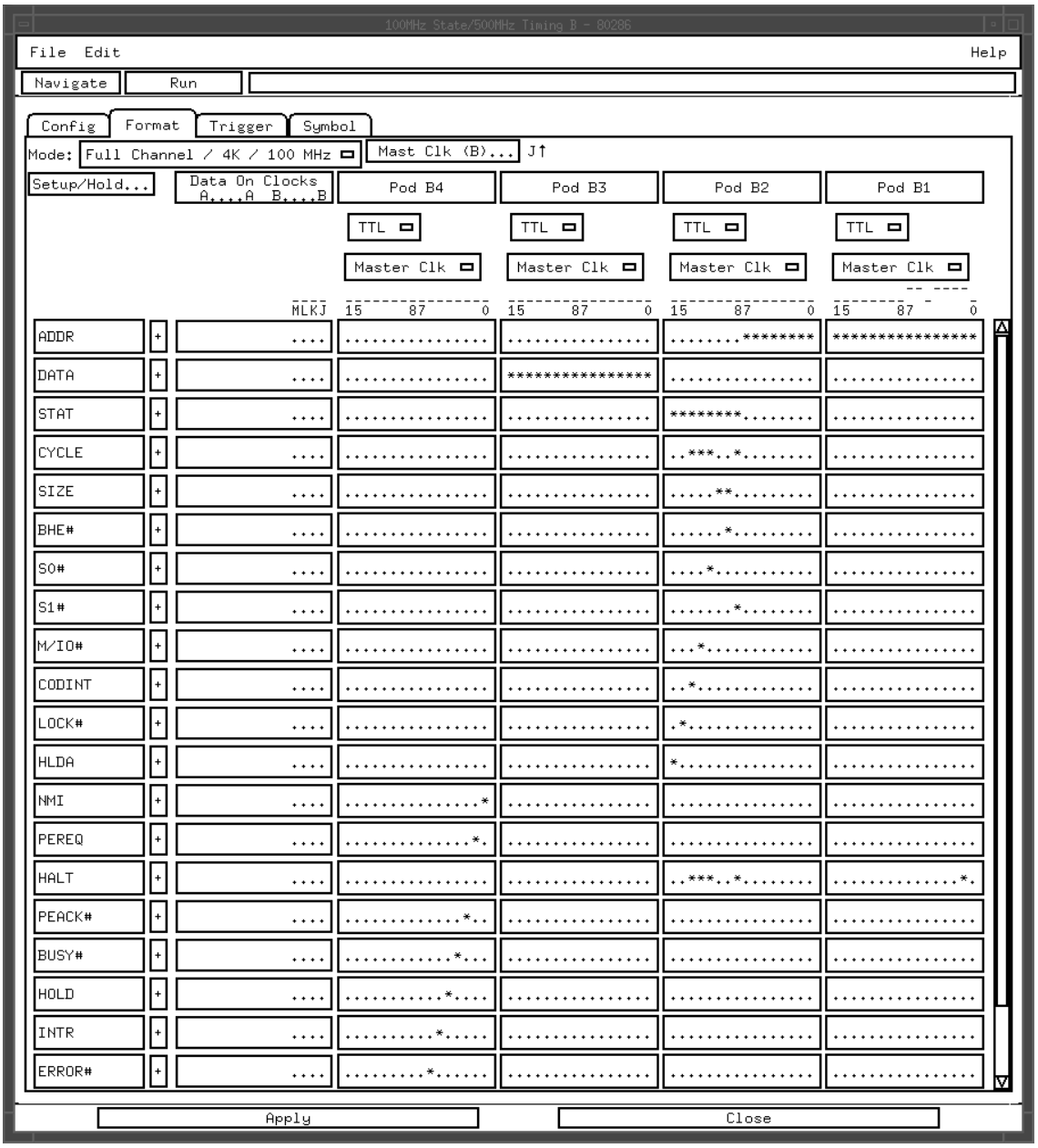
Format specification menu

The configuration files contain predefined format specifications. These format specifications include all labels for monitoring the microprocessor and any coprocessors connected directly to the microprocessor.

Chapter 4 of this guide contains a table that lists the signals for the 80286 processor, and on which pod and probe line the signal comes to the logic analyzer. Refer to this table in Chapter 4 and to the logic analyzer connection information for your analyzer in Chapter 2 to determine where the processor signals should be on the format specification screen.

Do not modify the ADDR, DATA, or STAT labels in the format specification if you want inverse assembly. Changes to these labels may cause incorrect or incomplete inverse assembly.

The following illustration shows the Format specification.



Format Specification

Status Encoding

Each of the bits of the STAT label are listed in the table below.

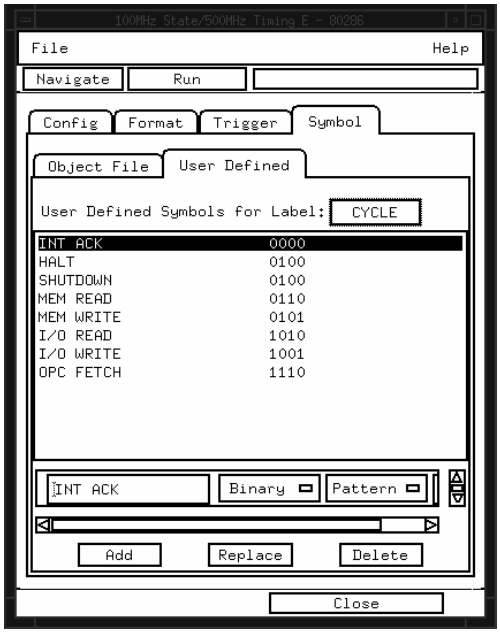
Status Label Bits

Status Bit	Signal Name
7	HLDA
6	LOCK#
5	COD/ IN
4	M/IO#
3	S0#
2	A0
1	BHE#
0	S1#

Logic Analyzer Symbols

The HP E2409C configuration software sets up symbol tables on the logic analyzer. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels have been defined in the format specification menu to make triggering on specific cycles easier. The label base in the symbols menu is set to hexadecimal to conserve space in the listing menu.

Select the Symbols field on the Format specification window and then choose a label name from the Label pop-up. The logic analyzer will display the symbols associated with the label. The figure on the following page shows the symbols for the CYCLE label.



CYCLE Symbols

The following table lists the label and symbol encodings defined by the logic analyzer configuration software.

80286 Symbol Table

Label	Symbol	Status Bit 7 6 5 4 3 2 1 0	A1
Cycle	INT ACK	x x 0 0 0 x x 0	
	HALT/SHUTDOWN	x x 0 1 0 x x 0	
	MEM READ	x x 0 1 1 x x 0	
	MEM WRITE	x x 0 1 0 x x 1	
	I/O READ	x x 1 0 1 x x 0	
	I/O WRITE	x x 1 0 0 x x 1	
	OPC FETCH	x x 1 1 1 x x 0	

Label	Symbol	Pod 4 8 7 6 5 4 3 2 1 0	A1
Halt	SHUTDOWN HALT	x x 0 1 0 x x 0 x x 0 1 0 x x 0	0
Size	WORD LSB MSB	x x x x x 0 0 x x x x x x 0 1 x x x x x x 1 0 x	
HLDA	CPU DMA	0 x x x x x x x 1 x x x x x x x	
BHE#	HI BYTE --	x x x x x x 0 x x x x x x x 1 x	
M/IO#	IO MEM	x x x 0 x x x x x x x 1 x x x x	
COD/IN	MEM CODE	x x 0 x x x x x x x 1 x x x x x	
LOCK#	LOCK --	x 0 x x x x x x x 1 x x x x x x	
S0#	S0 --	x x x x 0 x x x x x x x 1 x x x	
S1#	S1 --	x x x x x x x 0 x x x x x x x 1	
BUSY#	BUSY --	x x 0 x x x x x x x 1 x x x x x	
READY#	READY --	0 x x x x x x x x 1 x x x x x x x x	
ERROR#	ERROR --	x x 0 x x x x x x x x 1 x x x x x x	
RESET	-- RESET	x 0 x x x x x x x x 1 x x x x x x x	

Note: x = don't care

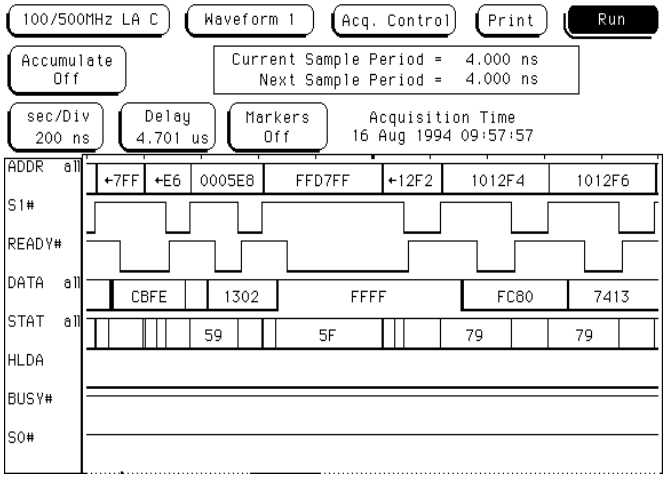
To display captured timing data

Select the Waveform menu for your logic analyzer. In the waveform menu, select the signals which you would like to view. Select run for a new acquisition.

Monitoring S0#, S1#, and READY# gives a complete picture of the bus cycles. The address and data information shown is the actual data which appears on the bus. Notice that they may fluctuate within a bus cycle because the information is required to be valid only within a short time period determined by the 80286 CPU specification.

Chapter 4 of this guide contains a table that lists the signals for the HP E2409C analysis probe and on which analysis probe pod and probe line the signal comes to the logic analyzer. Refer to this table and to the logic analyzer connection information in Chapter 2 to determine where the processor signals should be on the timing format specification screen.

The following figure shows the Waveform Menu display:



Timing Waveforms

The 80286 analysis probe contains two inverse assemblers, I80286S and I80286SE. I80286SE contains all the functions of the I80286S inverse assembler, plus additional features. For information on the I80286SE features, see "The I80286SE inverse assembler" on page 3-20.

The configuration software checks the logic analyzer during the load process. If the logic analyzer has the appropriate software version, the configuration file loads the enhanced inverse assembler. For information on the logic analyzer operating system version requirements, refer to "Logic analyzer software version requirements" on page 1-5.

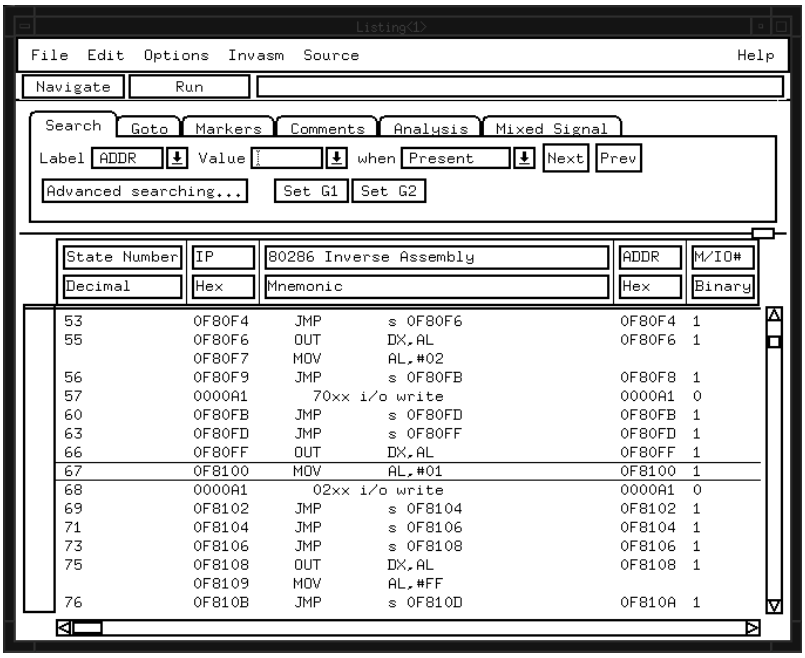
The following sections describe the features common to both inverse assemblers.

To display captured state data

Captured data is displayed as shown below with the I80286S inverse assembler, or as shown on the next page with the I80286SE inverse assembler. These figures display the state listing after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly language source code.

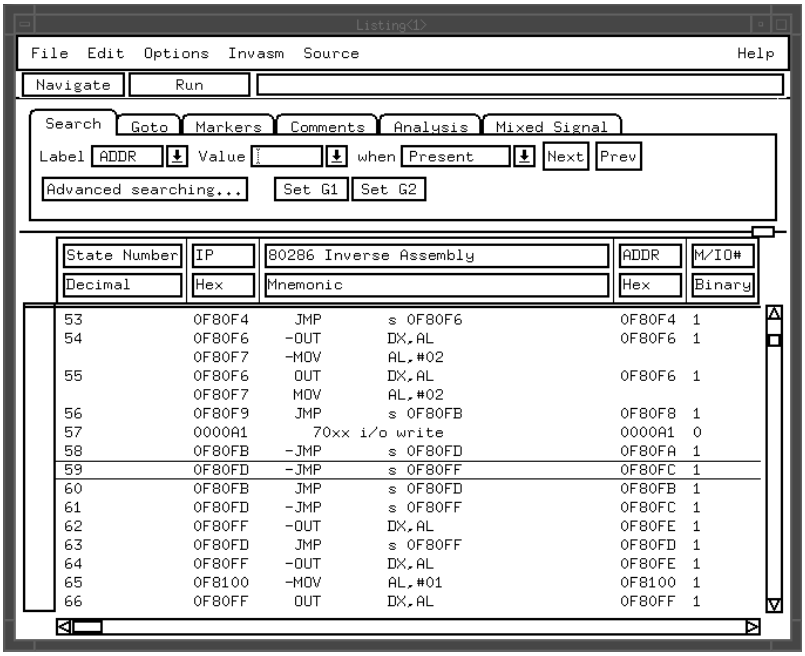
When the 80286 fetches a word (two bytes), instructions may begin on either or both bytes. The left-hand column of the IA display gives the least significant digit of the starting address of the instruction displayed. This is helpful in correlating analyzer traces with assembly listings.

If your trace listing doesn't otherwise appear to be correct (capturing the same RAM address twice, for example), make sure the analysis probe hardware is configured for state analysis, i.e. "jumper off." The "Invasm" field will appear at the top of the Listing Menu screen when the logic analyzer is configured for state analysis. See Chapter 2 to review the hardware configuration. Correct it if needed and run the trace again.



State Listing, I80286S Inverse Assembler

The following figure shows the Listing menu display using the I80286SE enhanced inverse assembler configured to suppress unused prefetches:



State Listing, I80286SE Inverse Assembler

To align the inverse assembler

The 80286 microprocessor does not indicate externally which byte fetched is the beginning of a new instruction. You may have to "point" to the first state of an instruction fetch to align the inverse assembler. Once aligned, the inverse assembler will disassemble from this state through the end of the screen.

Use the following procedure to align the inverse assembler:

1. Select a line on the display that you know contains the first byte of an instruction fetch.
2. Roll this line to the top of the display.

> Do not roll the instruction to the line number field at the left center screen. In the State Listing, I80286SE Inverse Assembler, line 53 is the top of the display.

3. Select the appropriate field for your inverse assembler or analyzer.
   a. For the HP 16600/700 series analyzers, select "Invasm," then select "Align." A pop-up menu appears with the following choices:

      Even Byte

      Odd Byte

   b. For the I80286SE inverse assembler on other analyzers, select "Invasm Options" and use the "Code Synchronization" submenu. The Code Synchronization submenu offers a toggle field with the following choices:

      Even Byte

      Odd Byte

   c. For the I80286S inverse assembler, select the "Invasm" field at the top of the display. A pop-up menu appears with the following choices:

      High

      Low
4. Select the choice that identifies which byte of the captured state contains the first byte of the code fetch.
5. Select "Align" to align the code.

The listing inverse assembles from the top line down. Any data before the top of the display is left unchanged.

Rolling the display up inverse assembles the lines as they appear on the bottom of the display. If you jump to another area of the display by entering a new line number, you may need to re-align the inverse assembler by repeating steps 1 through 5.

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

Inverse assembler output format

The next few paragraphs describe the general output format of the inverse assemblers.

Numeric Format

Unless a value is followed by a suffix character, numeric output from the inverse assembler is in hexadecimal format. For example, decimal values have a period (.) as the suffix character; binary values have a percent sign (%).

Multiple Instructions In a Single Fetch

Up to two instructions may be displayed for a single analyzer state, because the 80286 can fetch a word with two instruction bytes from program memory. When a single state contains more than one instruction, each instruction will be displayed on a separate line.

Multiple-Byte Instructions

Because an instruction may begin in any byte position, the last byte(s) of a multiple-byte instruction may extend into the lower byte(s) of the next word fetched. When interpreting a given state, the inverse assembler will ignore the byte(s) used by a previous instruction and will only display instructions that begin in that state.

Missing Opcodes

Asterisks (*) in the inverse assembler output indicate that a portion of an instruction was not captured by the analyzer. Missing opcodes occur frequently and are primarily due to microprocessor prefetch activity. Storage qualification, or the use of storage windows, can also lead to such occurrences.

Don’t Care Bytes

The 80286 microprocessor can perform byte and word transfers between microprocessor registers and memory. Byte transfers can occur in either byte on the 16-bit data bus. The bytes that are valid in a transfer are indicated by the microprocessor lines. The inverse assembler displays "xx" for any bytes in a transfer that are ignored by the microprocessor. You can determine exactly which byte or bytes of data were used as an operand.

Unexecuted Prefetched Instructions

The analysis probe sends all of the bus transactions by both the microprocessor and coprocessor to the logic analyzer. Prefetched instructions which are not executed by the microprocessor are marked by a hyphen "-".

In some cases, it is impossible to determine from bus activity whether a branch is taken or a prefetch is executed. In these cases, the inverse assembler marks the disassembled line with the prefix "?".

Unwanted Triggers

The logic analyzer captures prefetches, even if they are not executed. Care must be taken when you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microprocessor only prefetches at most three words, one technique to avoid unwanted triggering from unused prefetches is to add "6" to the trigger address. This trigger condition will only be satisfied if the branch is not taken.

Logical Address Display

Physical, rather than logical addresses, are used to perform symbolic address mapping. Most instructions, however, specify a 16-bit intrasegment offset and may indicate a segment different from the default segment for that particular instruction. Since the physical address cannot be determined from this information alone, the inverse assembler attempts to locate the resulting bus cycle so that the physical address may be obtained. If a bus cycle of the type indicated by the initiating instruction is not found, the physical address cannot be determined and an unmapped logical address (segment override, if any, and the 16-bit intrasegment offset) is displayed instead of a mapped physical address.

Instruction Type

The 80286 instruction set contains groups of instructions defining the instruction type in the second opcode byte, rather than in the first byte. In this case, if the second opcode byte is not stored in analyzer memory, only the group where an instruction resides can be determined. Therefore, the group name, rather than an instruction mnemonic, is displayed in the mnemonic display field. These group names are defined as follows:

Immed	Contains the following instructions when used with immediate source operands:	
	ADD	AND
	OR	SUB
	ADC	XOR
	SBB	CMP
Shift	Contains the following logical and arithmetic shifts and rotates:	
	ROL	SHL/SAL
	ROR	HR
	RCL	AR
	RCR	
Grp_1	Contains the following instructions:	
	TEST	MUL
	NOT	DIV
	NEG	IDIV
	MUL	
	The TEST instruction is included only when the instruction concerns an immediate source operand.	
Grp_2	Contains the following groups of instructions:	
	INC	when the instruction concerns memory operands on 8-bit registers
	DEC	when the instruction concerns memory operands on 8-bit registers
	CALL	indirect operand
	JMP	indirect operand
	PUSH	when the instruction concerns 16-bit memory operands
2-byte	Contains the following instructions or groups of instructions:	
	LAR	2 byte Grp1
	LSL	2 byte Grp2
	CLTS	

The 80286 instruction set contains two groups of instructions where the instruction type is defined in the third byte. In this case, if the third byte is not stored in analyzer memory, only the group where an instruction resides can be determined. Therefore, the group name, rather than an instruction mnemonic, is displayed in the mnemonic display field. These groups are defined as follows:

2 byte Grp1	Contains the following instructions:	
	SLDT	LTR
	STR	VERR
	LLDT	VERW
2 byte Grp2	Contains the following instructions:	
	SGDT	LGDT
	SIDT	LIDT
	SMSW	LMSW

Abbreviations

Listed below are several abbreviations for normal programming syntax that have been adopted to reduce the width of the inverse assembler display field.

dwp	DWORD PTR
wp	WORD PTR
bp	BYTE PTR
fp	FAR PTR
np	NEAR PTR
s	SHORT

These symbols are displayed only if the operation size cannot be determined from the instruction itself.

To further reduce the field width of the inverse assembler, LOCK and REPeat prefixes appear on the line before the instruction to which they apply.

Inverse assembler error messages

Any of the following list of error messages may appear during analysis of your target software. Included with each message is a brief explanation.

Illegal Task Request Displayed if the inverse assembler is used with an instrument other than the supported logic analyzers.

Fatal Data Error Displayed if the trace memory could not be read properly on entry into the inverse assembler.

Invalid Status Displayed if the status field for the current state is not valid.

Illegal Opcode Displayed if the inverse assembler encounters an illegal instruction.

Reserved Opcode Displayed if the inverse assembler encounters a reserved coprocessor instruction.

No Operand Displayed if the inverse assembler cannot find a complete operand field for an instruction. Prefetch activity or storage qualification is often the cause.

The I80286SE inverse assembler

The I80286SE inverse assembler contains all the functions of the I80286S inverse assembler (see previous sections), plus additional features that use the increased capabilities of some of the logic analyzers. For the enhanced inverse assembler, the logic analyzer must meet the software version requirements listed in "Logic analyzer software version requirements" on page 1-5.

The Invasm menu contains three functions: Load (HP 16600/700 only), Filtering with Show/Suppress selections, and Align. The following sections describe these functions.

Load

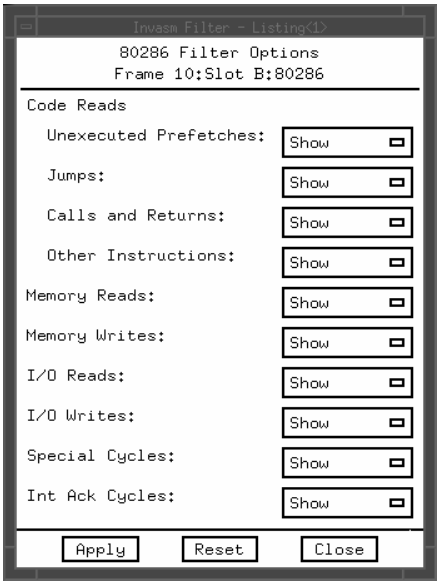
The Load function lets you load a different inverse assembler and apply it to the data in the Listing menu. In some cases you may have acquired raw data, in which case the Load function lets you apply an inverse assembler to that data.

Filter

The Filter function brings up a Show/Suppress menu (see figure on following page). You can change the settings to specify whether the various microprocessor operations are shown or suppressed on the logic analyzer display. The preceding figure shows the microprocessor operations which have this option. The settings for the various operations do not affect the data which is stored by the logic analyzer. The settings only affect whether that data is displayed or not. The same data can be examined with different settings for different analysis requirements.

This function gives you a better analysis display in two ways. First, unneeded information can be filtered out of the display. For example, you can suppress the display of unexecuted prefetches that might clutter up the display but that do not provide any meaningful information.

Second, some particular operations can be isolated by suppressing all other operations. For example, I/O accesses can be shown, with all other operations suppressed to allow for quick analysis of I/O accesses.



Filter Menu

If the X or O pattern markers are turned on, and the designated pattern is found in a state that has been Suppressed with display filtering, the following message will appear on the logic analyzer display: "X (or O) pattern found, but state is suppressed."

Align

Align enables the inverse assembler to re-align with the microprocessor code. In some cases the prefetch marking algorithm in the inverse assembler may lose synchronization, and unused prefetches or executed instructions may be incorrectly marked. If any of the Code Reads are suppressed, this could cause some executed instructions to be missing from the display.

To align the inverse assembler, use the procedure described earlier.

Coprocessor Support

The HP E2409C analysis probe and inverse assembler fully supports the 80287 math coprocessor instructions.

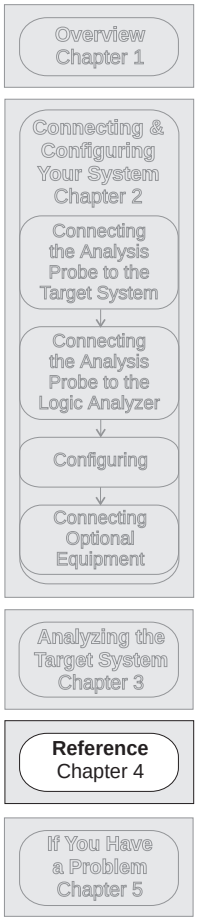
Reference

Reference

This chapter contains additional reference information including the signal mapping for the HP E2409C Analysis Probe.

The information in this chapter is presented in the following sections:

- Operating characteristics of the analysis probe
- Theory of operation and clocking
- Signal-to-connector mapping
- Circuit board dimensions
- Replaceable parts



Operating characteristics of the analysis probe

The following operating characteristics are not specifications, but are typical operating characteristics for the analysis probe.

Operating Characteristics

Microprocessor Compatibility	Intel 80286 microprocessor, and all microprocessors made by other manufacturers that comply with Intel 80286 specifications.
Microprocessor Package	68-pin contact PGA. 68-pin contact PLCC (with option 1CB adapters).
Accessories Required	Option 1CB for PLCC target systems.
Logic Analyzer Required	HP 1660A/AS/C/CS/CP, HP 1661A/AS/C/CS/CP, HP 1662A/AS/C/CS/CP, HP 1670A/D, HP 1671A/D, HP 1672A/D, HP 16550A (one card), HP 16554A/55A/56A (one card), HP 16555D/56D (one card), HP 16600A, HP 16601A, HP 16602A, HP 16603A.
Probes Required	Four pods of signals are available. Three pods are required for inverse assembly.
Maximum Clock Speed	25 MHz clock output (50 MHz clock input).
Power Requirements	1.0 A at +5 Vdc maximum from the logic analyzer. CAT I, Pollution degree 2.
Signal Line Loading	All signals have approximately 8 pF load except for RESET and HLDA, which have 16 pF load.
Timing Analysis	All signals are buffered by 74FCT646ATQ gates with a 1-ns channel-to-channel skew except for S0 and S1. S0 and S1 are buffered twice and have a 5-ns delay relative to all other signals.

Operating Characteristics

Environmental Temperature	Operating	0 to 55 degrees C (+32 to +131 degrees F)
	Non-operating	-40 to +75 degrees C (-40 to +167 degrees F)
Altitude	Operating	4,600 m (15,000 ft.)
	Non-operating	15,300 m (50,000 ft.)
Humidity	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

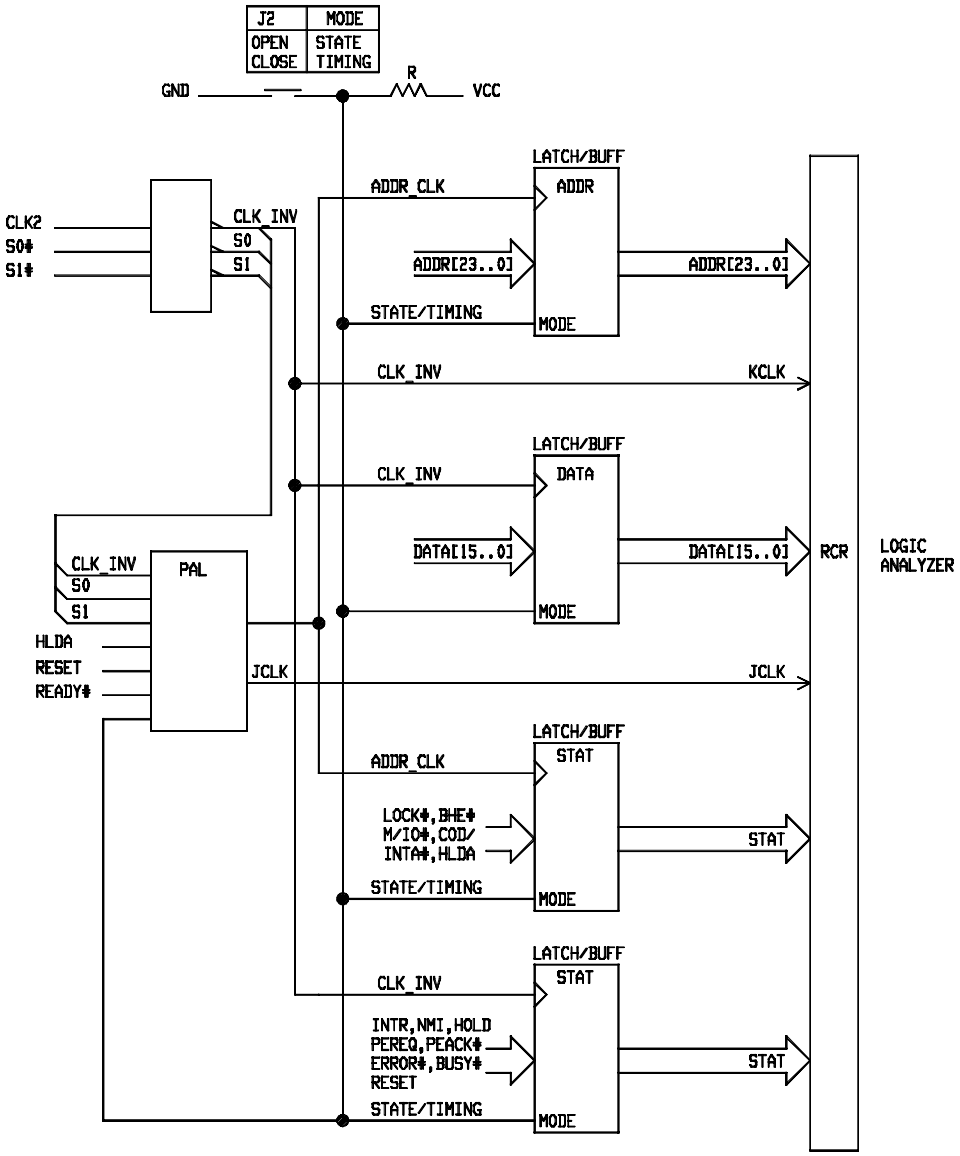
Theory of operation and clocking

State-per-transfer mode is the default mode in the configuration software. In State-per-transfer mode, the address bus latches on the CPU clock after S0# & S1# become valid. The address information is held there until the next assertion of S0# and S1#. The PAL monitors READY# after S0# & S1# are asserted. If READY# gets asserted, the PAL generates a master clock to the logic analyzer which captures the address, data, and status from the latch.

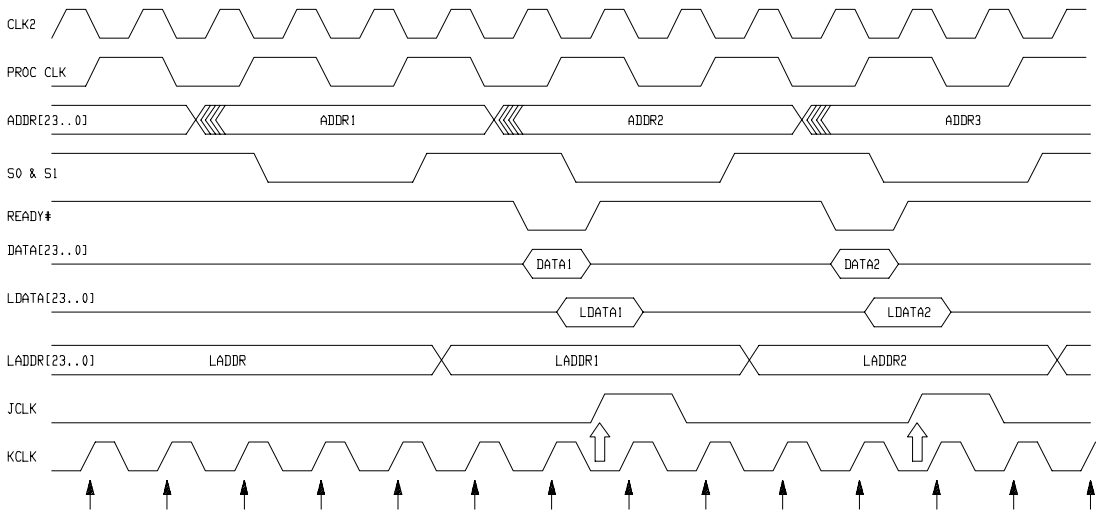
In State-per-clock mode, everything is the same except that a master clock is generated for each falling edge of the CPU input clock. This mode is useful if you need to see the changes in the data and status bus on each CPU clock. To switch to this mode, install the jumper on the analysis probe, then change the clock in the format menu from "J rising edge" to "K rising edge". Each "K clock rising edge" corresponds to a falling edge of the CPU input clock. The data and status bus are latched on every rising edge of the CPU clock.

The analysis probe also allows the logic analyzer to operate in Timing mode. Switching from State to the Timing mode requires adding a jumper on the analysis probe hardware. It also requires changing the software setting in the configuration menu from State to Timing. In this mode, all signals flow straight through and nothing gets latched. The rate of sampling varies depending upon the type of HP logic analyzer used, ranging from 100 MHz to 250 MHz.

The figure on page 4-5 shows a block diagram of the HP E2409C analysis probe. The figure on page 4-6 shows a timing diagram representing when the analysis probe latches address and data.



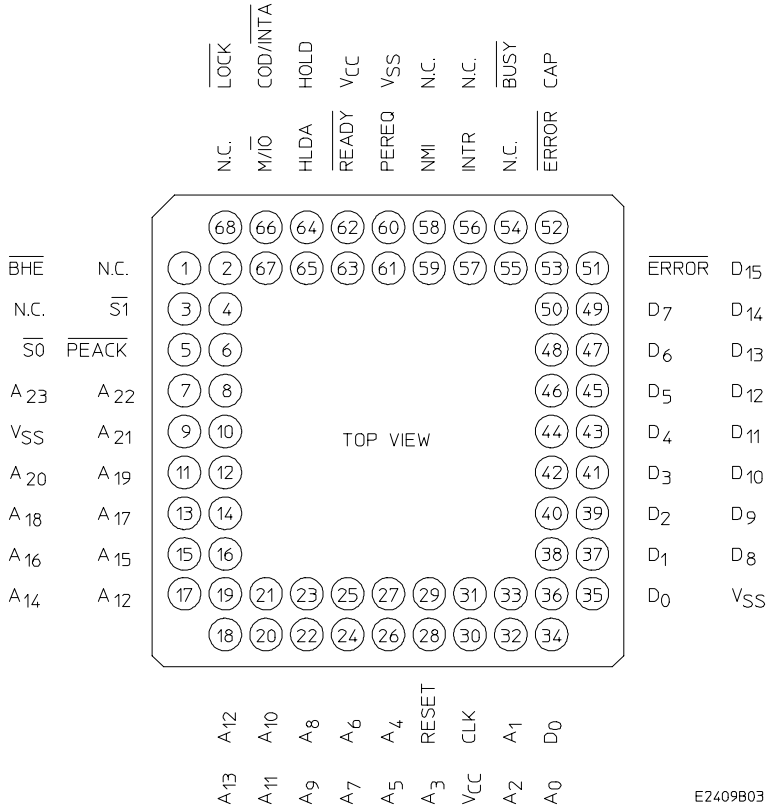
Block Diagram



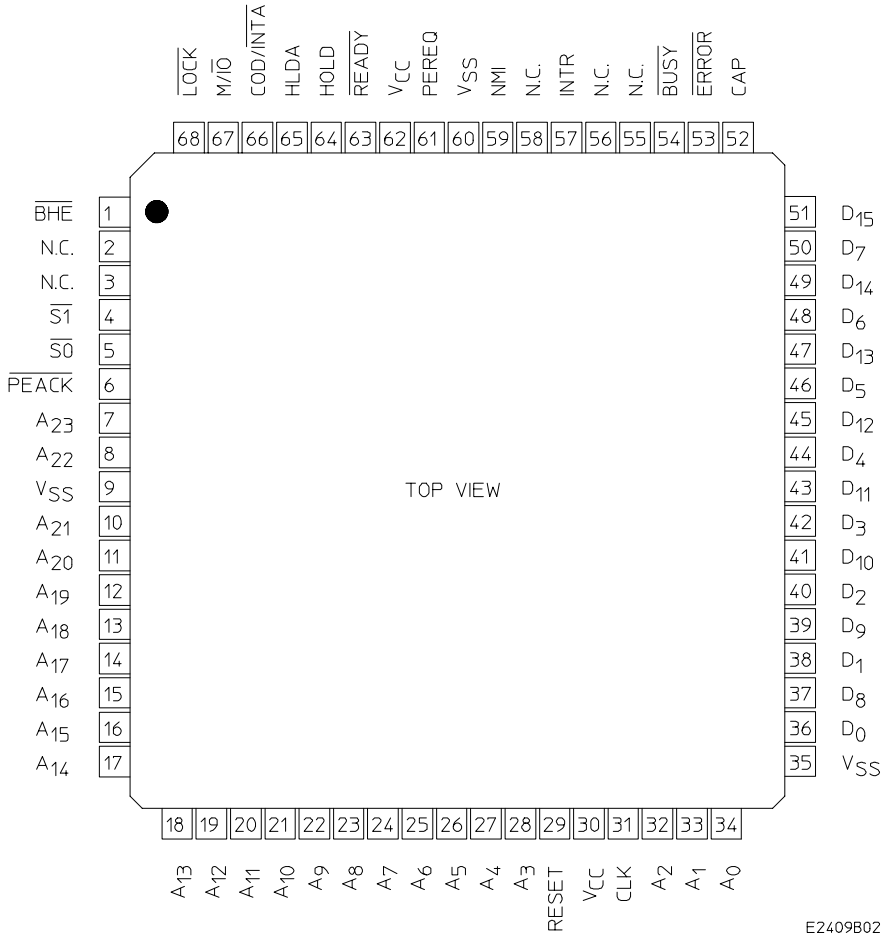
Timing Diagram

Signal-to-connector mapping

The following figures show the analysis probe PGA socket pin mapping and the PLCC microprocessor package, respectively. The following table shows the signal-to-connector mapping.



80286 68-Pin PGA Socket Diagram
Top View



80286 68-Pin PLCC Socket Diagram
Top View

The signal list table column descriptions are as follows:

POD	The analysis probe pod the signal that carries the signal.
LA PROBE	The probe within the pod that carries the signal.
PIN MNE	The processor mnemonic for the pin.
PGA PIN	The PGA pin number.
LABEL	The analyzer label assigned to the signal.

80286 Signal List

POD	LA PROBE	PIN MNE	PGA PIN	LABEL	ALT LABEL
P1	0	A0	34	ADDR	
P1	1	A1	33	ADDR	
P1	2	A2	32	ADDR	
P1	3	A3	28	ADDR	
P1	4	A4	27	ADDR	
P1	5	A5	26	ADDR	
P1	6	A6	25	ADDR	
P1	7	A7	24	ADDR	
P1	8	A8	23	ADDR	
P1	9	A9	22	ADDR	
P1	10	A10	21	ADDR	
P1	11	A11	20	ADDR	
P1	12	A12	19	ADDR	
P1	13	A13	18	ADDR	
P1	14	A14	17	ADDR	
P1	15	A15	16	ADDR	

80286 Signal List

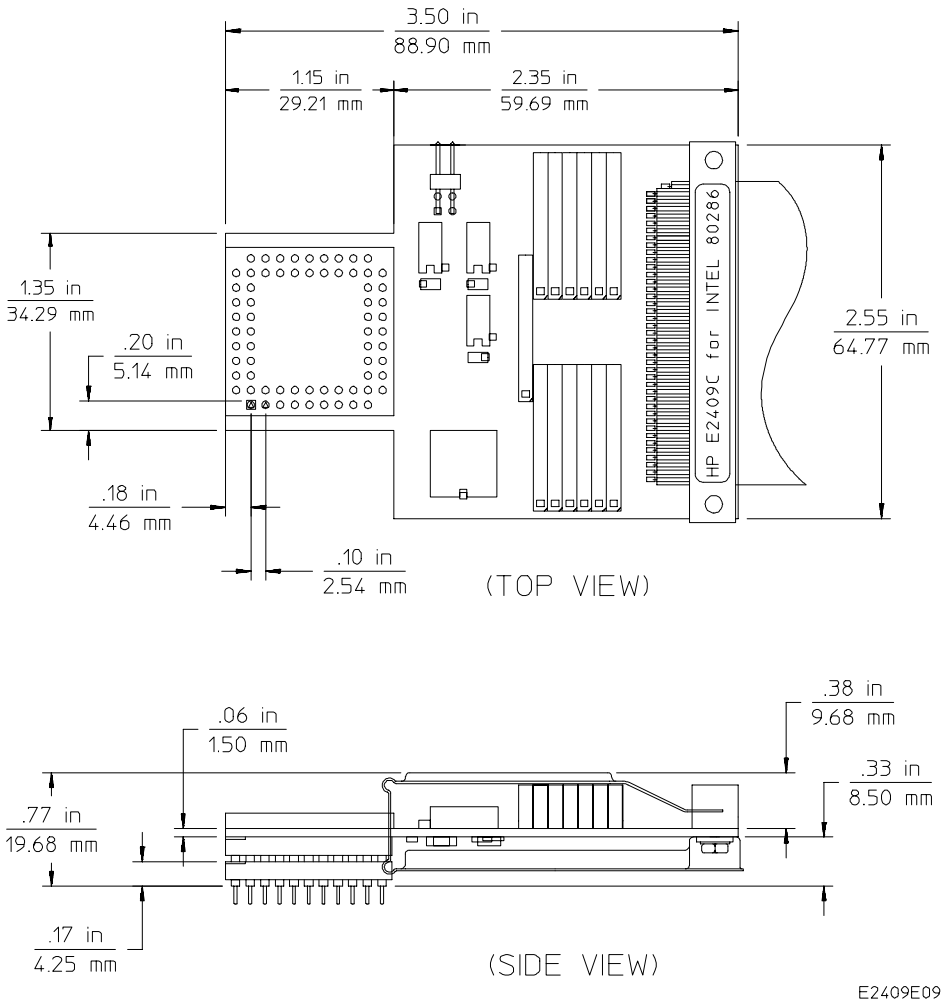
POD	LA PROBE	PIN MNE	PGA PIN	LABEL	ALT LABEL
P2	0	A16	15	ADDR	
P2	1	A17	14	ADDR	
P2	2	A18	13	ADDR	
P2	3	A19	12	ADDR	
P2	4	A20	11	ADDR	
P2	5	A21	10	ADDR	
P2	6	A22	8	ADDR	
P2	7	A23	7	ADDR	
P2	8	S1#	4	STAT	S1#
P2	9	BHE#	1	STAT	BHE#
P2	10	A0	34	STAT	
P2	11	S0#	5	STAT	S0#
P2	12	M/IO#	67	STAT	M/IO#
P2	13	COD/INTA#	66	STAT	CO/IN#
P2	14	LOCK#	68	STAT	LOCK#
P2	15	HLDA	65	STAT	HLDA
P3	0	D0	36	DATA	
P3	1	D1	38	DATA	
P3	2	D2	40	DATA	
P3	3	D3	42	DATA	
P3	4	D4	44	DATA	
P3	5	D5	46	DATA	
P3	6	D6	48	DATA	
P3	7	D7	50	DATA	
P3	8	D8	37	DATA	
P3	9	D9	39	DATA	
P3	10	D10	41	DATA	
P3	11	D11	43	DATA	
P3	12	D12	45	DATA	
P3	13	D13	47	DATA	
P3	14	D14	49	DATA	
P3	15	D15	51	DATA	

80286 Signal List

POD	LA PROBE	PIN MNE	PGA PIN	LABEL	ALT LABEL
P4	0	NMI	59	NMI	
P4	1	PEREQ	61	PEREQ	
P4	2	PEACK#	6	PEACK	
P4	3	BUSY#	54	BUSY#	
P4	4	HOLD	64	HOLD	
P4	5	INTR	57	INTR	
P4	6	ERROR#	53	ERROR#	
P4	7	RESET	29	RESET	
P4	8	READY#	63	READY#	
P4	9	N/C			
P4	10	N/C			
P4	11	N/C			
P4	12	N/C			
P4	13	N/C			
P4	14	N/C			
P4	15	N/C			

Circuit board dimensions

The following figure gives the dimensions for the analysis probe assembly. The dimensions are listed in inches and millimeters.



Circuit Board Dimensions

Replaceable parts

The repair strategy for this analysis probe is board replacement. However, the table below lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales Office for further information on servicing the board.

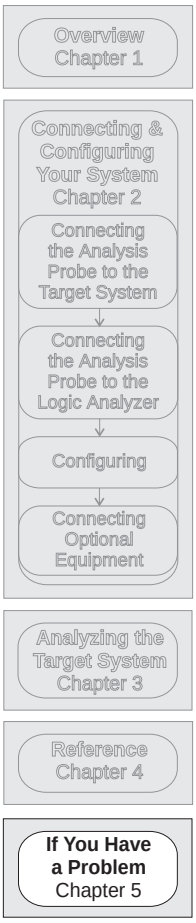
Exchange assemblies are available when a repairable assembly is returned to Hewlett-Packard. These assemblies have been set up on the "Exchange Assembly" program. This lets you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Replaceable Parts

HP Part Number	Description
E2409-69504	Exchange Board Assembly
1200-1516	Pin Protector IC Socket
5081-7703	PGA-PLCC Adapter
E2409-68705	Disk Pouch Software Package

If You Have a Problem

If You Have a Problem



Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

The information in this chapter is presented in the following sections:

- Logic analyzer problems
- Analysis probe problems
- Inverse assembler problems
- Intermodule measurement problems
- Messages
- Cleaning the instrument

If you still have difficulty after trying the suggestions in this chapter, contact your local Hewlett-Packard Service Center.

CAUTION

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and analysis probes. Otherwise, you may damage circuitry in the analyzer, analysis probe, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ☐ **Remove and reseat all cables and probes, ensuring that there are no bent pins on the analysis probe or poor probe connections.**
- ☐ **Adjust the threshold level of the data pod to match the logic levels in the system under test.**
- ☐ **Use an oscilloscope to check the signal integrity of the data lines.**

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also See "Capacitive loading" in this chapter for information on other sources of intermittent data errors.

Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

- ☐ **Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.**

  The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

No activity on activity indicators

- ☐ Check for loose cables, board connections, and analysis probe connections.
- ☐ Check for bent or damaged pins on the analysis probe.

No trace list display

If there is no trace list display, it may be that your trigger specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ☐ Check your trigger sequencer specification to ensure that it will capture the events of interest.
- ☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Analyzer won't power up

If the logic analyzer power is powered down when it is connected to a powered-up target system, the logic analyzer may not be able to power up. Some logic analyzers are inhibited from powering up when they are connected to a target system that is already powered up.

- ☐ Disconnect all logic analyzer cabling from the analysis probe. This will allow the logic analyzer to power up. Reconnect logic analyzer cabling after power up.

Analysis Probe Problems

This section lists problems that you might encounter when using an analysis probe. If the solutions suggested here do not correct the problem, you may have a damaged analysis probe. Contact your local Hewlett-Packard Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the analysis probe, the microprocessor (if socketed) or the analysis probe may not be installed properly, or they may not be making electrical contact.

- ☐ **Ensure that you are following the correct power-on sequence for the analysis probe and target system.**

  1 Power up the analyzer and analysis probe.

  2 Power up the target system.

  If you power up the target system before you power up the analysis probe, interface circuitry in the analysis probe may latch up and prevent proper target system operation.

- ☐ **Verify that the microprocessor and the analysis probe are properly rotated and aligned so that the index pin on the microprocessor (pin 1 or pin A1) matches the index pin on the analysis probe.**

- ☐ **Verify that the microprocessor and the analysis probe are securely inserted into their respective sockets.**

- ☐ **Verify that the logic analyzer cables are in the proper sockets of the analysis probe and are firmly inserted.**

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

- ☐ **Do a full reset of the target system before beginning the measurement.**

  Some analysis probe designs require a full reset to ensure correct configuration.

- ☐ **Ensure that your target system meets the timing requirements of the processor with the analysis probe installed.**

  See “Capacitive Loading” in this chapter. While analysis probe loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.

- ☐ **Ensure that you have sufficient cooling for the microprocessor.**

  Some microprocessors generate substantial heat. This is exacerbated by the active circuitry on the analysis probe board. You should ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the analysis probe, or system lockup in the microprocessor. All analysis probes add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

- ☐ **Remove as many pin protectors, extenders, and adapters as possible.**

- ☐ **If multiple analysis probe solutions are available, use one with lower capacitive loading.**

Inverse Assembler Problems

This section lists problems that you might encounter while using the inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the analysis probe or in your target system. If you follow the suggestions in this section to ensure that you are using the analysis probe and inverse assembler correctly, you can proceed with confidence in debugging your target system.

No inverse assembly or incorrect inverse assembly

This problem may be due to incorrect alignment, modified configuration files, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

- ☐ **Ensure that each logic analyzer pod is connected to the correct analysis probe connector.**

  There is not always a one-to-one correspondence between analyzer pod numbers and analysis probe cable numbers. Microprocessor interfaces must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order. The cable connections for each analysis probe are often altered to support that need. Thus, one analysis probe might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 2 for connection information.

- ☐ **Check the activity indicators for status lines locked in a high or low state.**

- ☐ **Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.**

  These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some analysis probes also require other data labels. See Chapter 3 for more information.

- ☐ **Verify that all microprocessor caches and memory managers have been disabled.**

  In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly. It may be incorrect because a portion of the execution trace was not visible to the logic analyzer.

- ☐ **Verify that storage qualification has not excluded storage of all the needed opcodes and operands.**

Inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

- ☐ **For the HP 16600/700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD ROM. Re-install the Processor Support Package for this product, then try loading the configuration file again.**

- ☐ **For other logic analyzers, ensure that the inverse assembler is on the same disk as the configuration files you are loading.**

  Configuration files for the state analyzer contain a pointer to the name of the corresponding inverse assembler. If you delete the inverse assembler, rename it, or use the File Manager Copy command to copy it to the HP 16600/700 logic analysis systems, the configuration process will fail to load the inverse assembler.

  See Chapter 3 for details.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

- **Adjust the skew in the Intermodule menu.**

  You may be able to specify a skew value that enables the event to be captured.

- **Change the trigger specification for modules upstream of the one with the problem.**

  If you are using a logic analyzer to trigger the scope, try specifying a trigger condition one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and may not always be related to the event you are trying to capture with the oscilloscope.

Analyzer Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Enhanced Inverse Assembler Not Found"

This error only occurs on the HP 16600/700 logic analysis systems. This error occurs if you rename or delete the enhanced inverse assembler file that is attached to the configuration file, or if you do not properly install the inverse assembler file on the hard disk. Ensure that the inverse assembler file is not renamed or deleted. If you use the File Manager Copy command to copy an inverse assembler to the HP 16600/700 logic analysis systems, the enhanced inverse assembler will not load. Use the Install procedures listed on the jacket of the CD ROM to install the files for this product.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

For the HP 16600/700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD ROM.

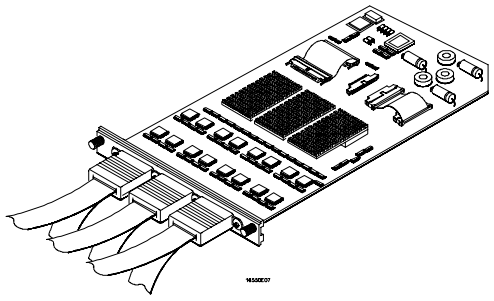
For other logic analyzers, if you have copied the files to the logic analyzer hard disk, ensure that the inverse assembler is located in the same directory as the configuration file.

". . . Does Not Appear to be an Inverse Assembler File"

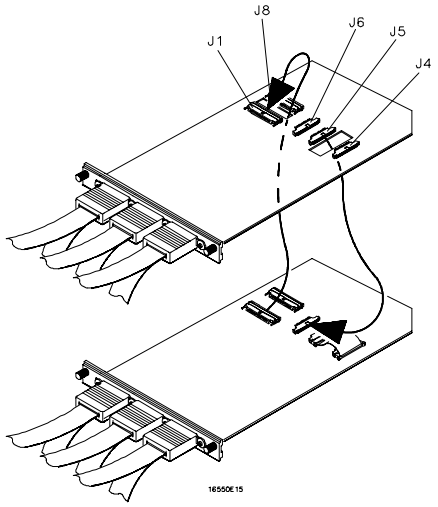
This error occurs if the inverse assembler file requested by the configuration file is not a valid inverse assembler. Use the Install procedures listed on the jacket of the CD ROM to re-install the files for this product.

"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly on logic analysis cards. The following diagrams show the correct cable connections for one-card and two-card HP 16550A installations. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.



Cable Connections for One-Card HP 16550A Installations

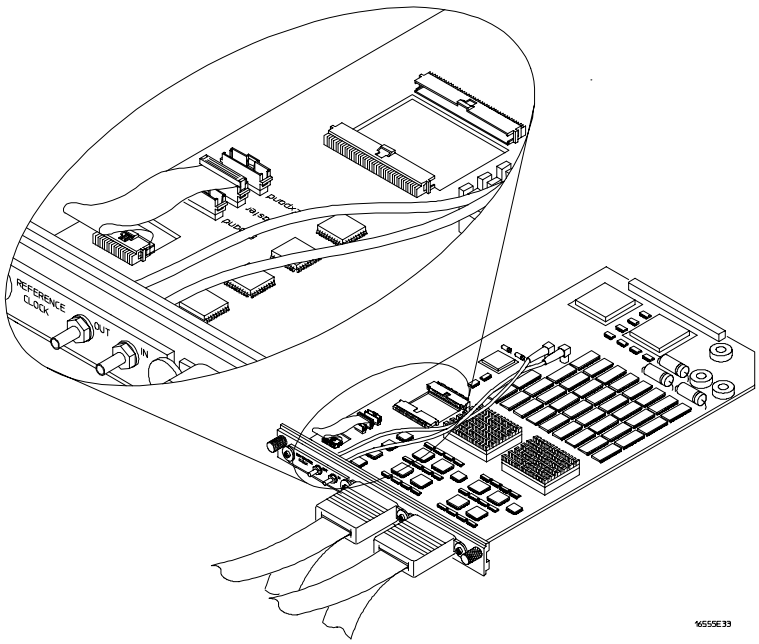


Cable Connections for Two-Card HP 16550A Installations

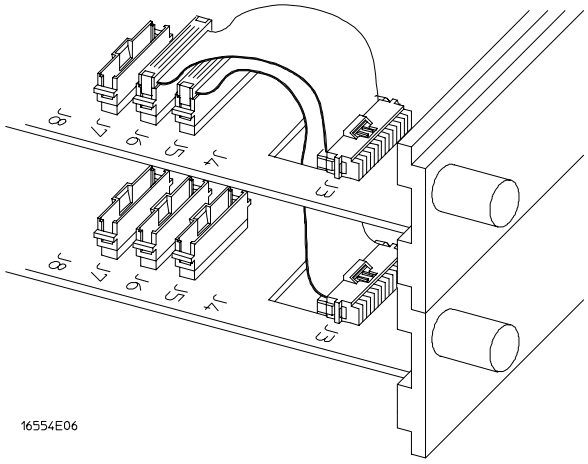
See Also

The *HP 16550A 100-MHz State/500-MHz Timing Logic Analyzer Service Guide*.

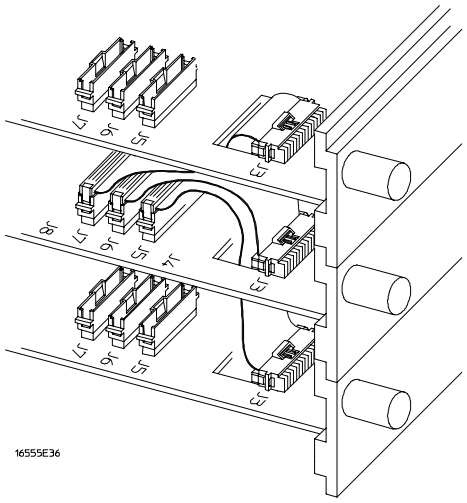
The following diagrams show the correct cable connections for one-card, two-card, and three-card installations on HP 16554A, HP 16555A/D, and HP 16556A/D logic analysis cards. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.



Cable Connections for One-Card HP 16554/55/56 Installations



Cable Connections for Two-Card HP 16554/55/56 Installations



Cable Connections for Three-Card HP 16554/55/56 Installations

See Also

The HP 16554A 70-MHz State/250-MHz Timing Logic Analyzer Service Guide.

The HP 16555A 110-MHz State/250-MHz Timing Logic Analyzer Service Guide.

The HP 16556A 100-MHz State/400-MHz Timing Logic Analyzer Service Guide.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ☐ Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A/B/C disk operation menu. Selecting Load {All} will cause incorrect operation when loading most analysis probe configuration files.

See Also Chapter 2 describes how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

- ☐ This error message might occur if the logic analyzer cards are not firmly seated in the logic analysis system mainframe. Ensure that the cards are firmly seated.
- ☐ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- ☐ If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the analysis probe. See Chapter 2 to determine the proper connections.

“Time from Arm Greater Than 41.93 ms”

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

“Waiting for Trigger”

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- When analyzing microprocessors that fetch only from word-aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a word boundary, the trigger will never be found.

Cleaning the Instrument

If this instrument requires cleaning, disconnect it from all power sources and clean it with a mild detergent and water. Make sure the instrument is completely dry before reconnecting it to a power source.

Glossary

Analysis Probe A probe connected to the target microprocessor. It provides an interface between the signals of the target microprocessor and the inputs of the logic analyzer.

Connector Board A board whose only function is to provide connections from one location to another. One or more connector boards might be stacked to raise a probe above a target micoprocessor to avoid mechanical contact with other components installed close to the target microprocessor.

Elastomeric Probe Adapter A connector that is fastened on top of a target microprocessor using a retainer and knurled nut. The conductive elastomer on the bottom of the probe adapter makes contact with pins of the target microprocessor and delivers their signals to connection points on top of the probe adapter.

Emulation Module An emulation module is installed within the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Probe.

Emulation Probe An emulation probe is a stand-alone instrument connected to the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Module.

Flexible Adapter Two connection devices coupled with a flexible cable. Used for connecting probing hardware on the target microprocessor to the analysis probe.

General-purpose Flexible Adapter A cable assembly that connects the signals from an elastomeric probe adapter to an analysis probe. Normally, a male-to-male header or transition board makes the connections from the general-purpose flexible adapter to the analysis probe.

High-Density Adapter Cable A cable assembly that delivers signals from an analysis probe hardware interface to the logic analyzer pod cables. A high-density adapter cable has a single Mictor connector that is installed into the analysis probe, and two cables that are connected to corresponding odd and even logic analyzer pod cables.

High Density Termination Adapter Cable Same as a High Density Adapter Cable, except it has a termination in the Mictor connector.

Jumper Moveable direct electrical connection between two points.

Mainframe Logic Analyzer A logic analyzer that resides on one or more board assemblies installed in an HP 16500B/C, 1660xA, or 16700A mainframe.

Male-to-male Header A board assembly that makes point-to-point connections between the female pins of a flexible adapter or transition board and the female pins of an analysis probe.

Preprocessor Interface See Analysis Probe.

Preprocessor Probe See Analysis Probe.

Probe adapter See Elastomeric Probe Adapter.

Processor Probe See Emulation Probe and Emulation Module.

Prototype Analyzer The HP 16505A prototype analyzer acts as an analysis and display processor for the HP 16500B/C logic analysis system. It provides a windowed interface and powerful analysis capabilities.

Setup Assistant A software program that guides you through the process of connecting and configuring an analysis probe and logic analyzer to make measurements on a specific microprocessor.

Shunt Connector. See Jumper.

Stand-alone Logic Analyzer A stand-alone logic analyzer has a predefined set of hardware components which provide a specific set of capabilities. It is designed to perform logic analysis. A stand-alone logic analyzer differs from a mainframe logic analyzer in that it does not offer card slots for installation of additional capabilities, and its specifications are not modified based upon selection from a set of optional hardware boards that might be installed within its frame.

Transition Board A board assembly that obtains signals connected to one side and re-arranges them in a different order for delivery at the other side of the board.

1/4-Flexible Adapter An adapter that obtains one-quarter of the signals from an elastomeric probe adapter (one side of a target microprocessor) and makes them available for probing.

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